

FM9B HANKS Intel UMA

VER : 3A

PWA:

PWB:

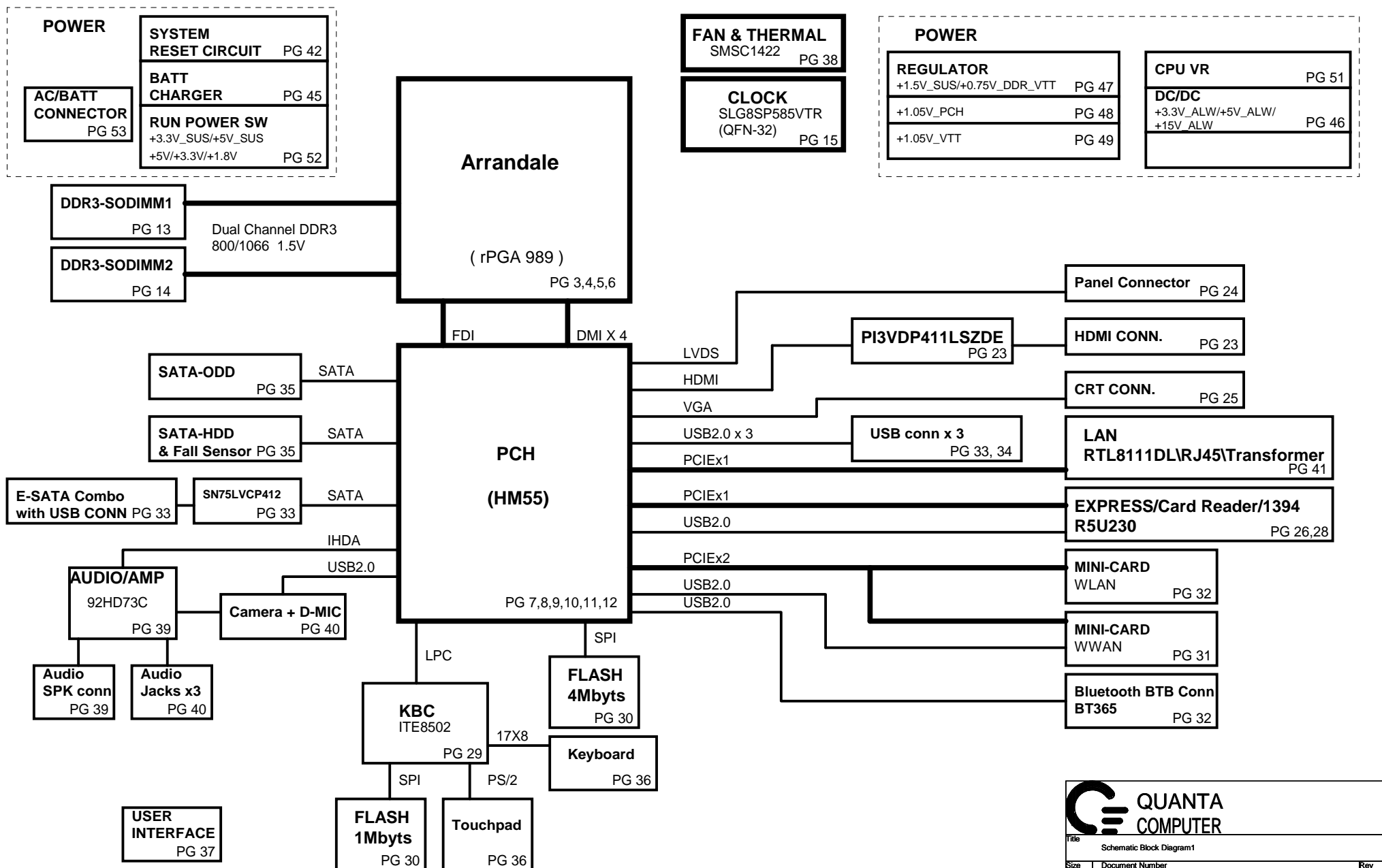



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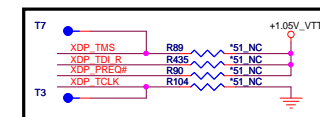
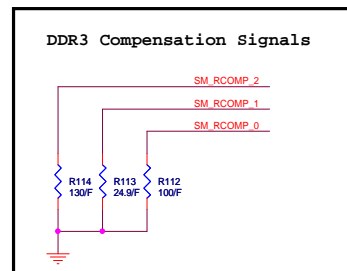
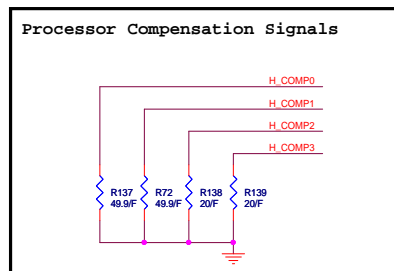
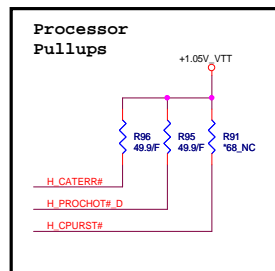
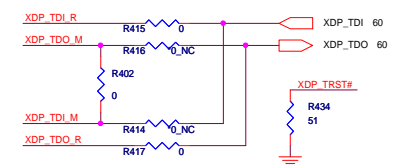
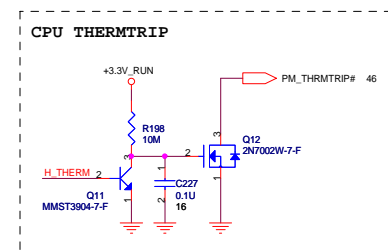
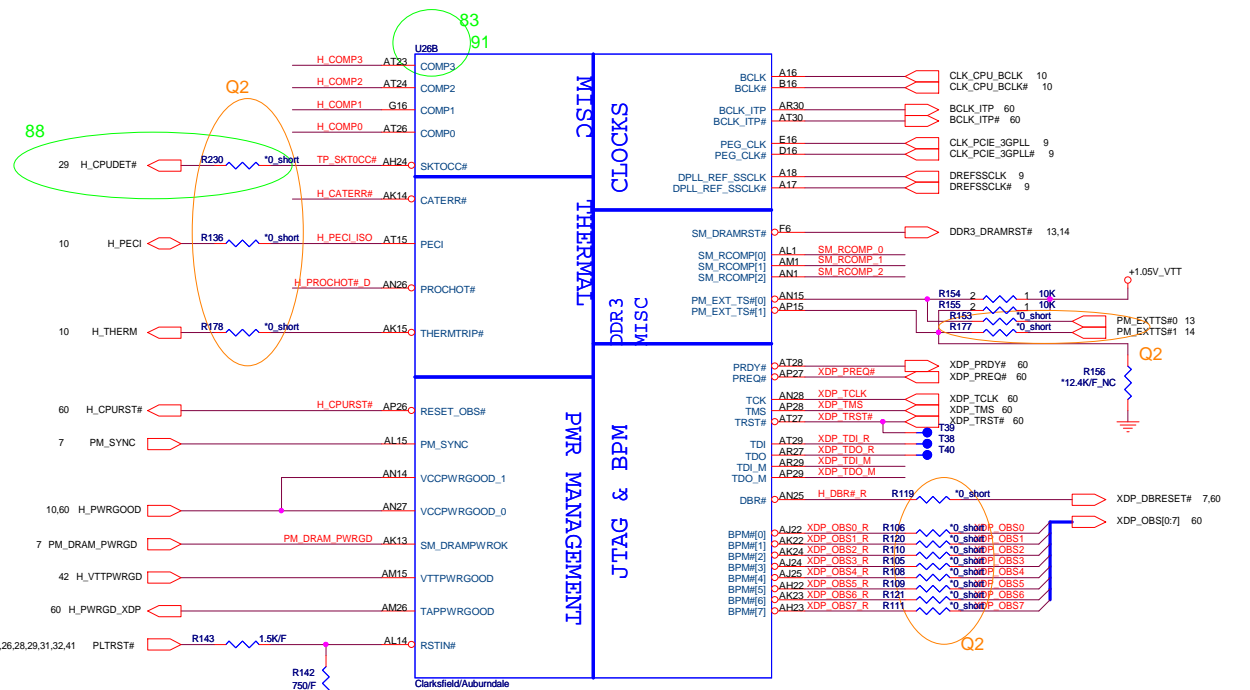
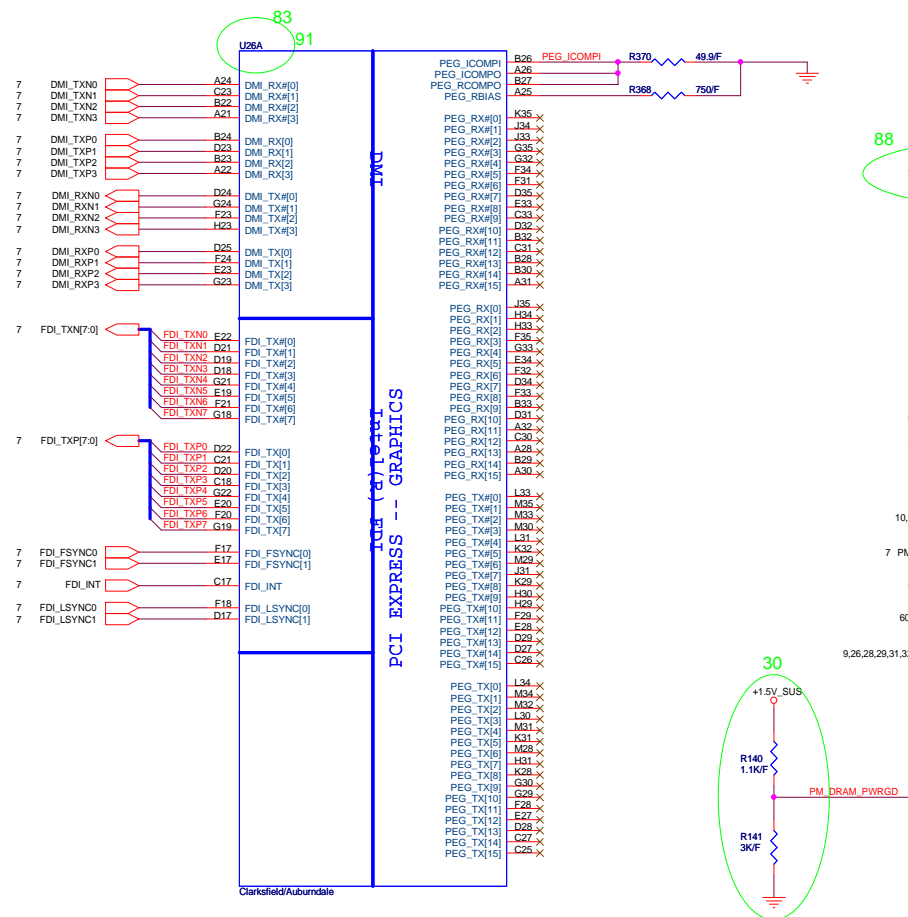
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.05V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,28,31,32,52	Express Card/Min Card	RUN_ON	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	

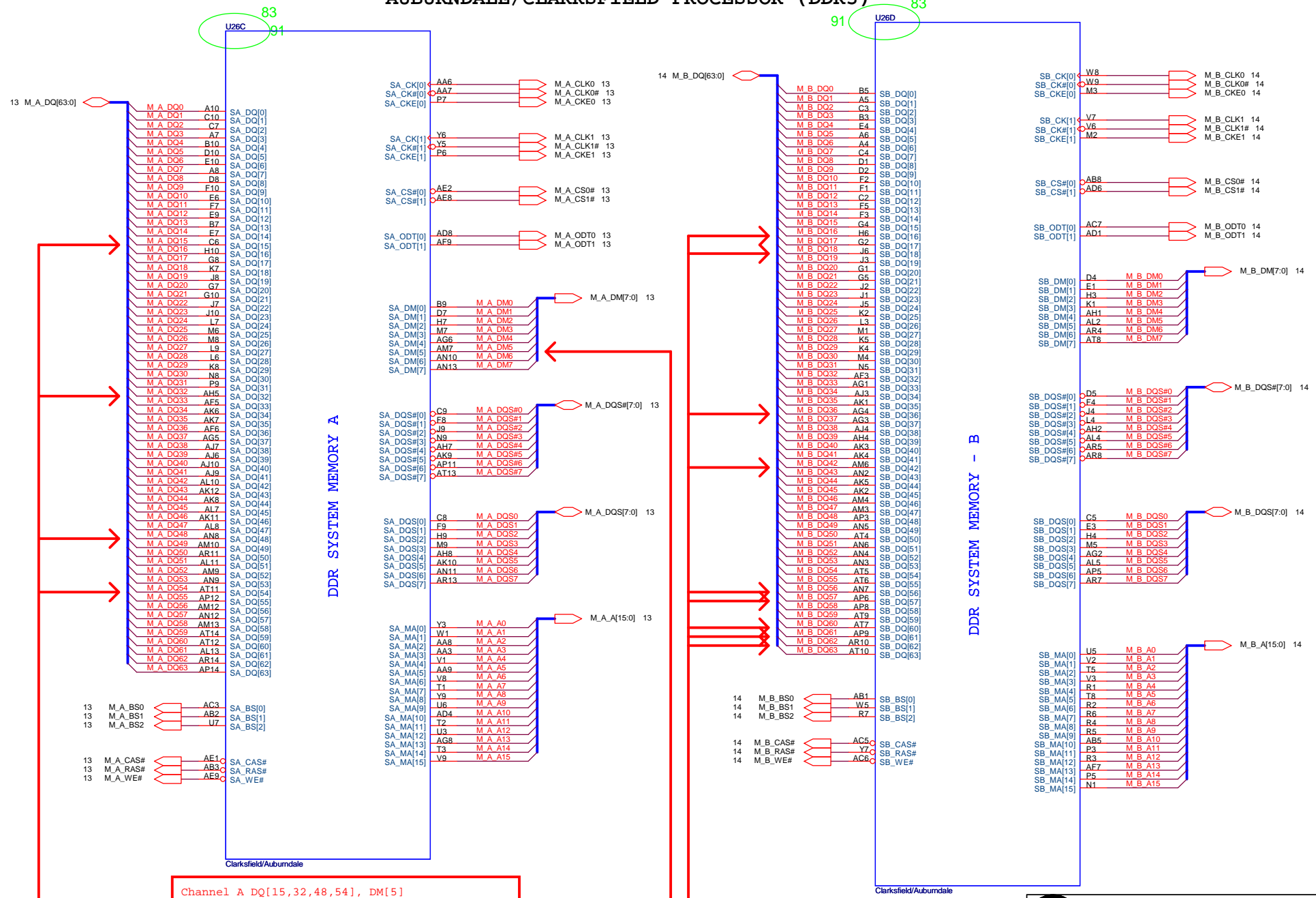
GND PLANE	PAGE	DESCRIPTION
 GND	ALL	

QUANTA
COMPUTER

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AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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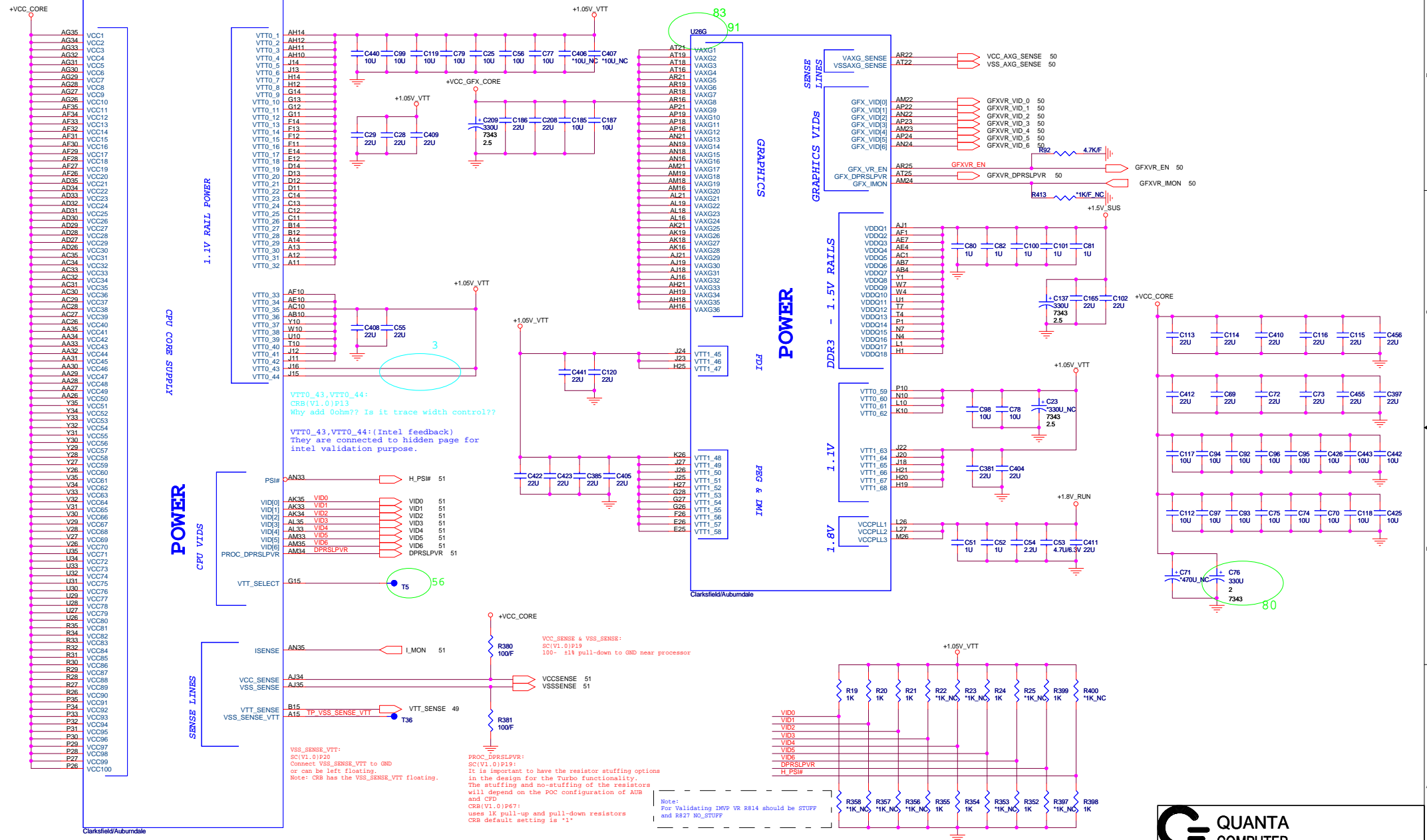
File: AUBURNDA 2/4

Size: Document Number
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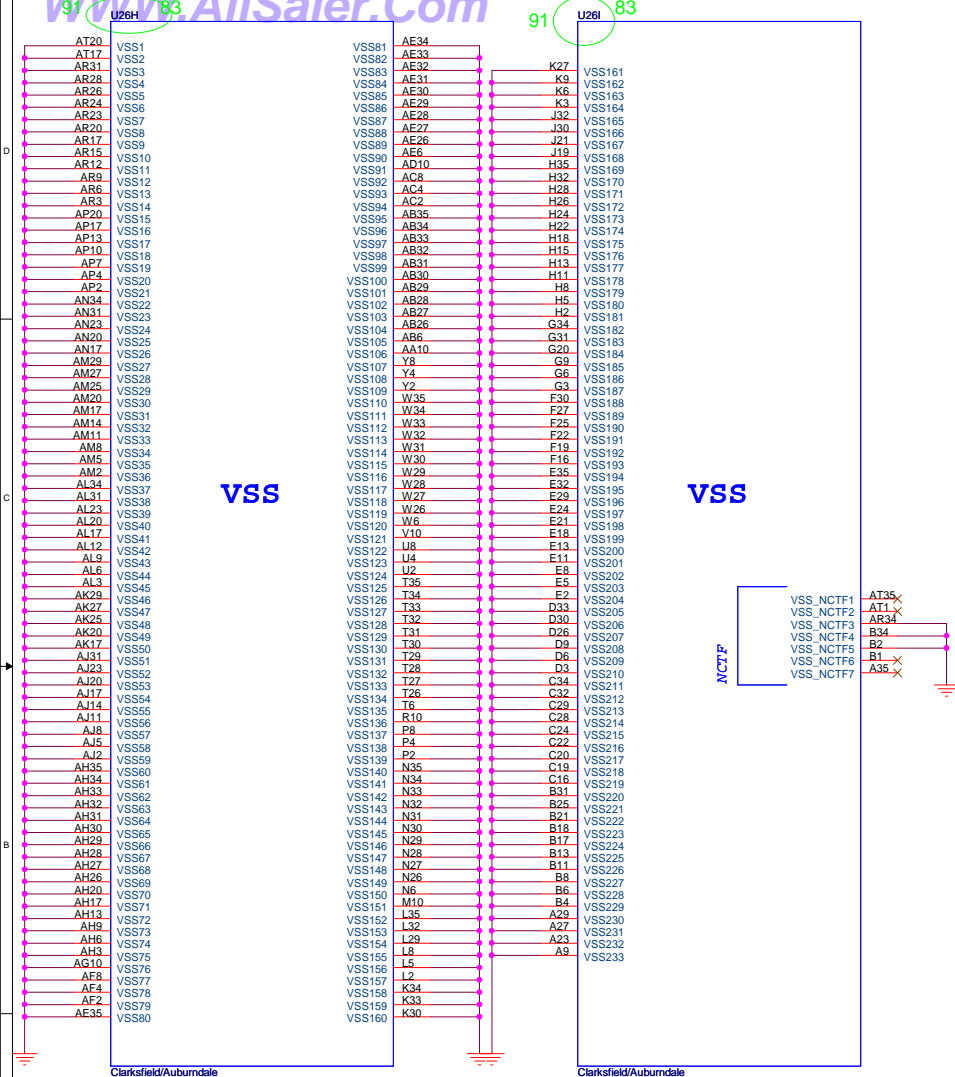
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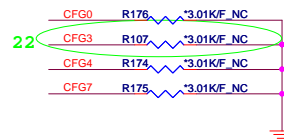


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

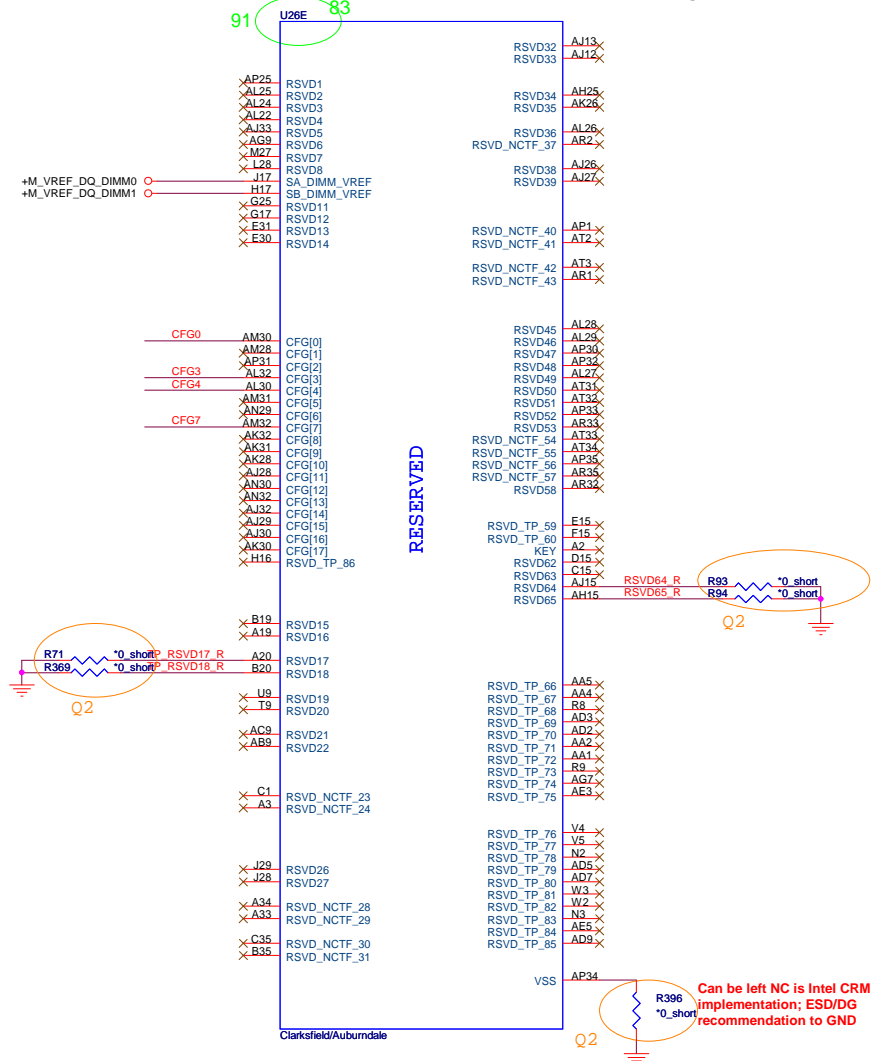
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



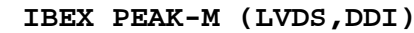
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

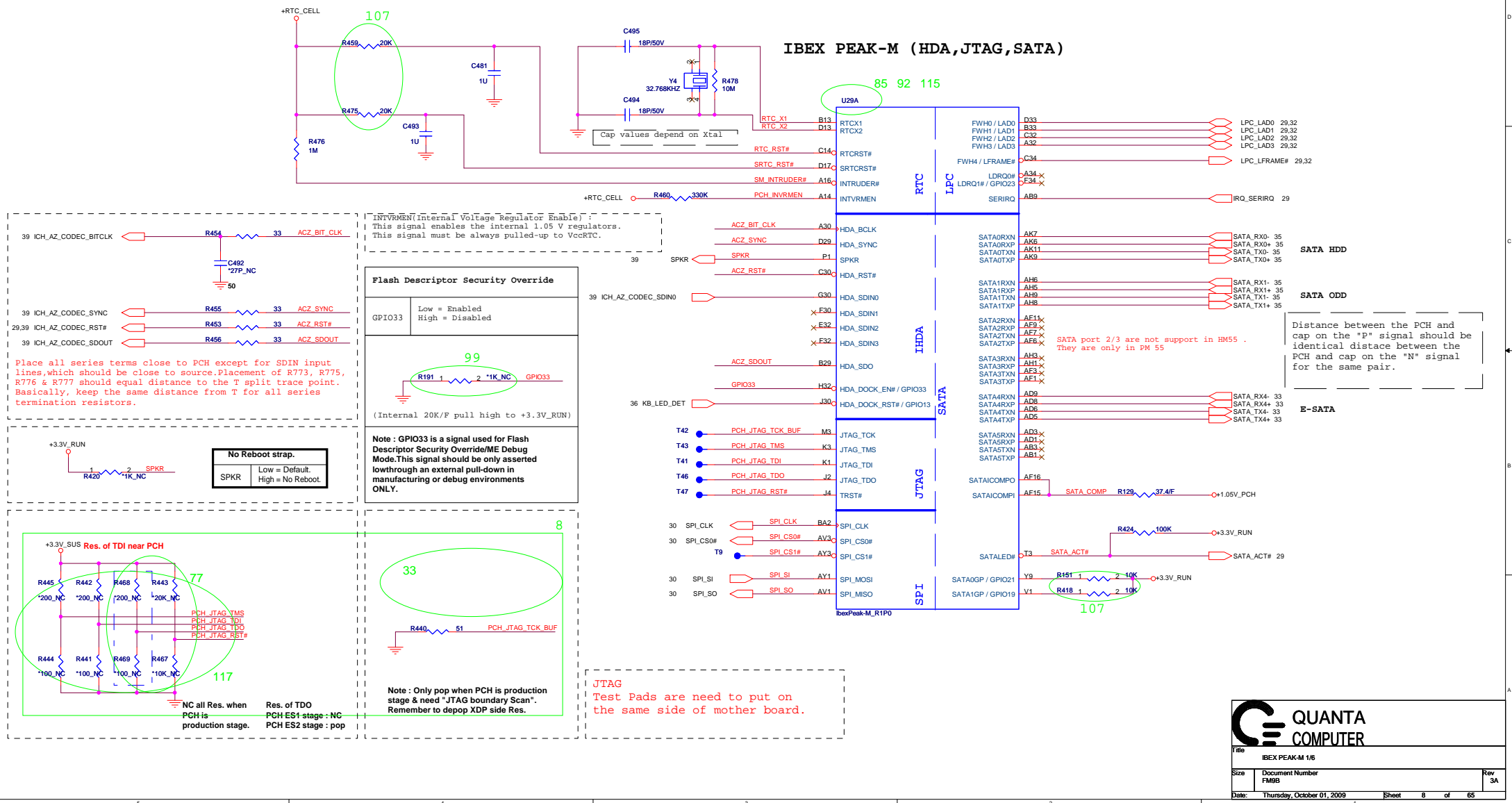
QUANTA COMPUTER

Title: AUBURND 4/4

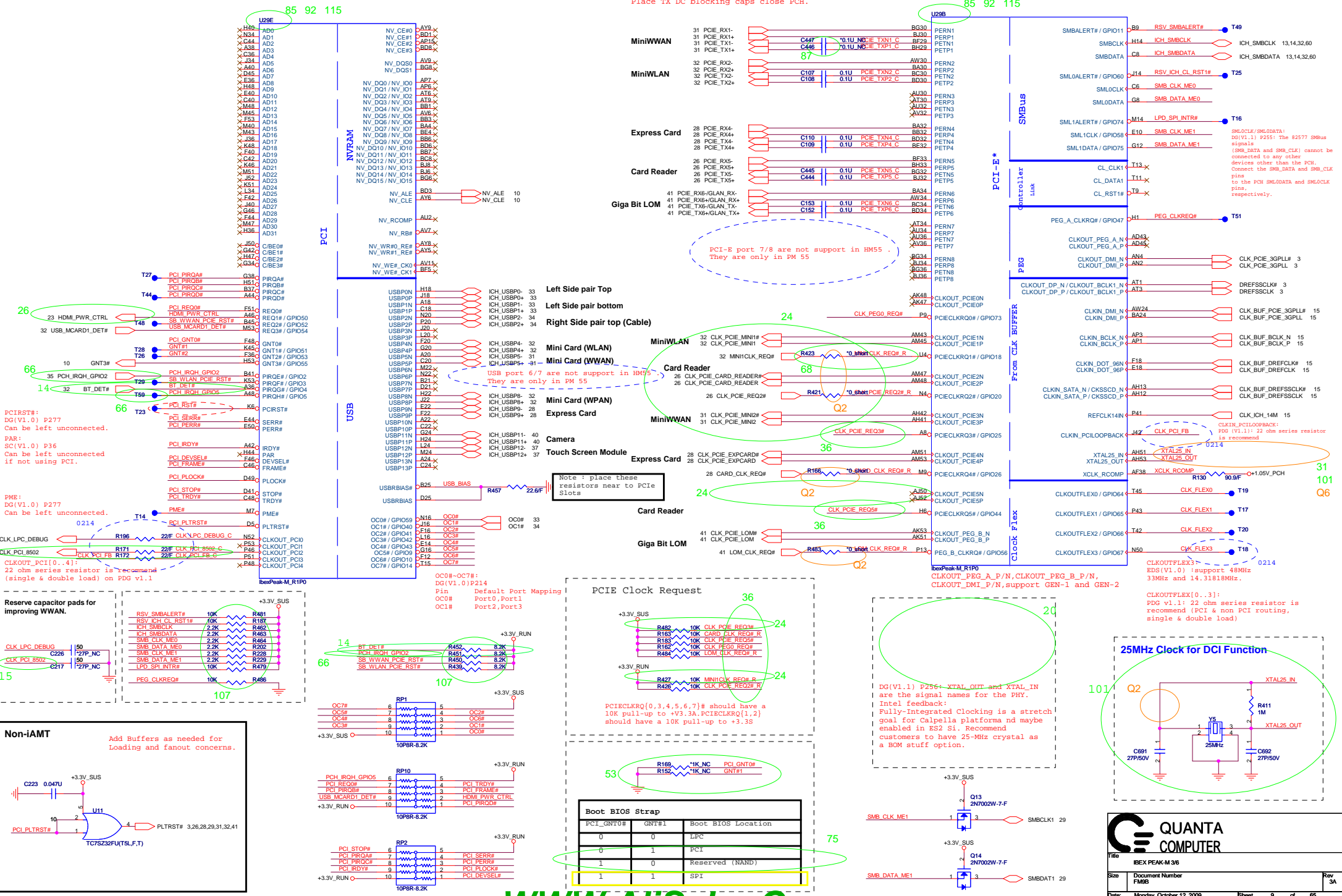
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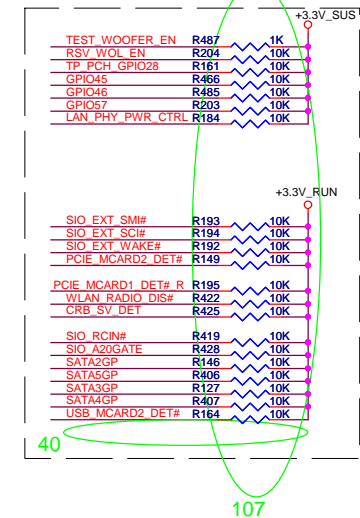
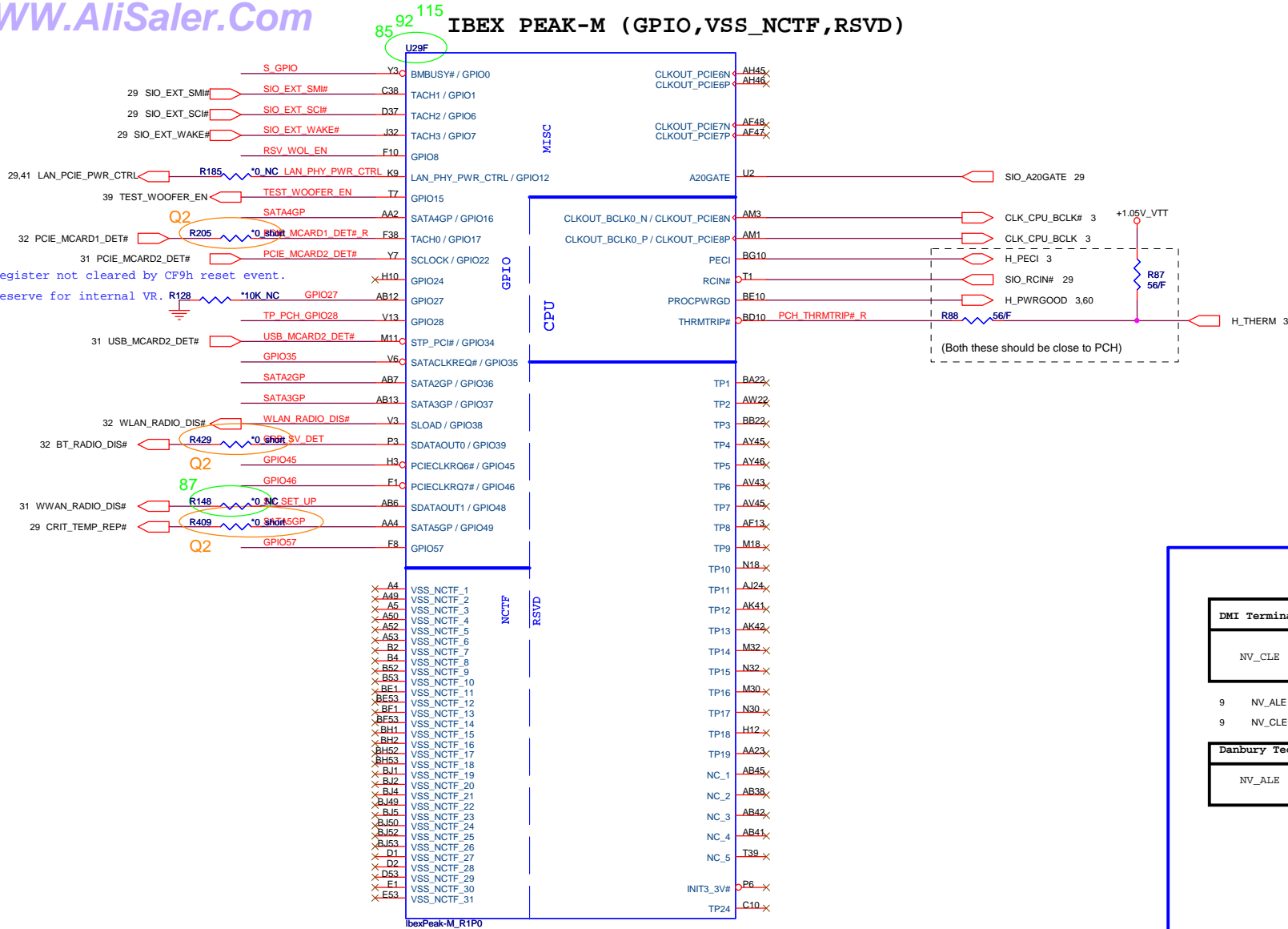




Place TX DC blocking caps close PCH.



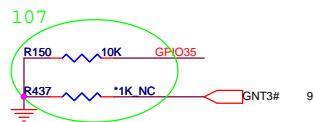
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



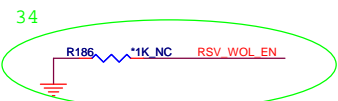
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH



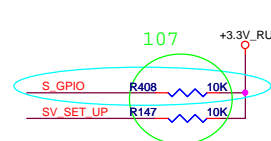
Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low Disable when sampled high



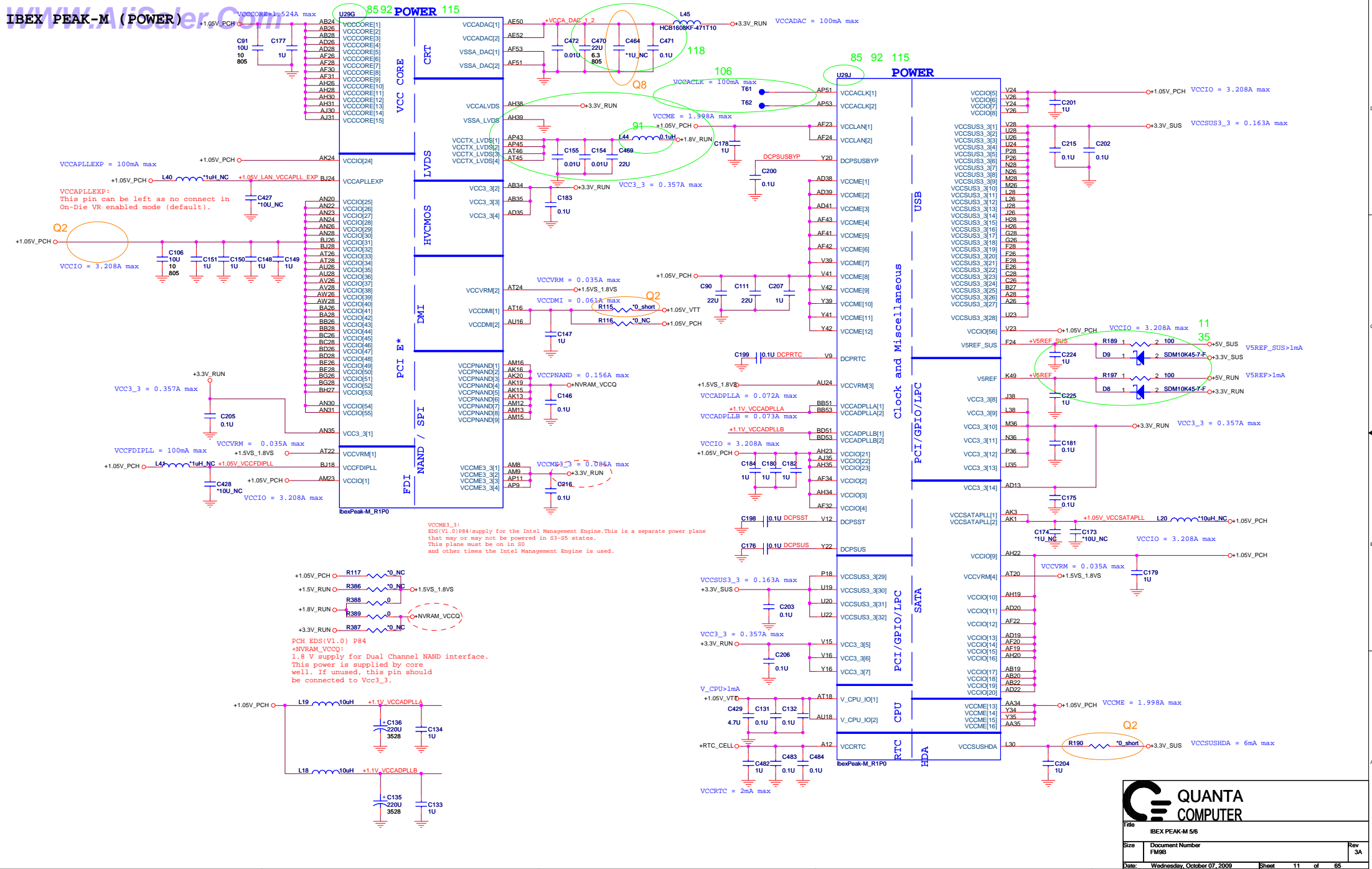
SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

BMBUS#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3.3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUS#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

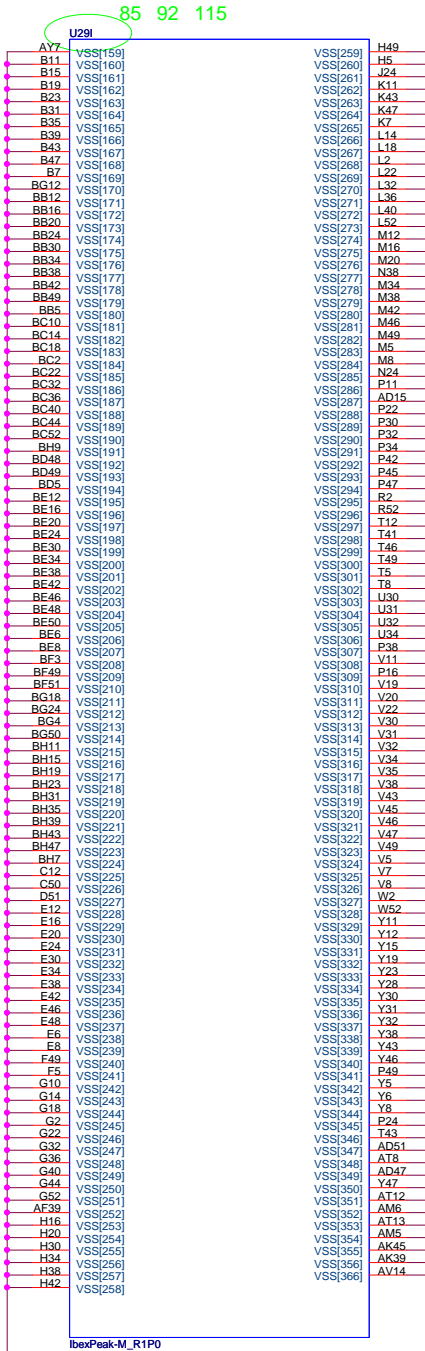
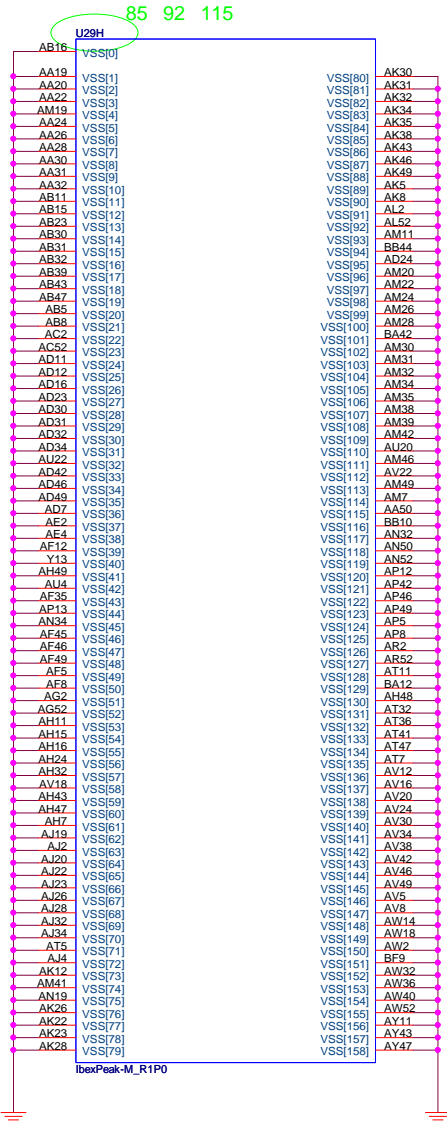



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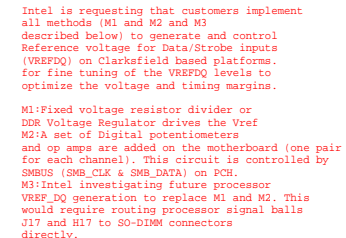


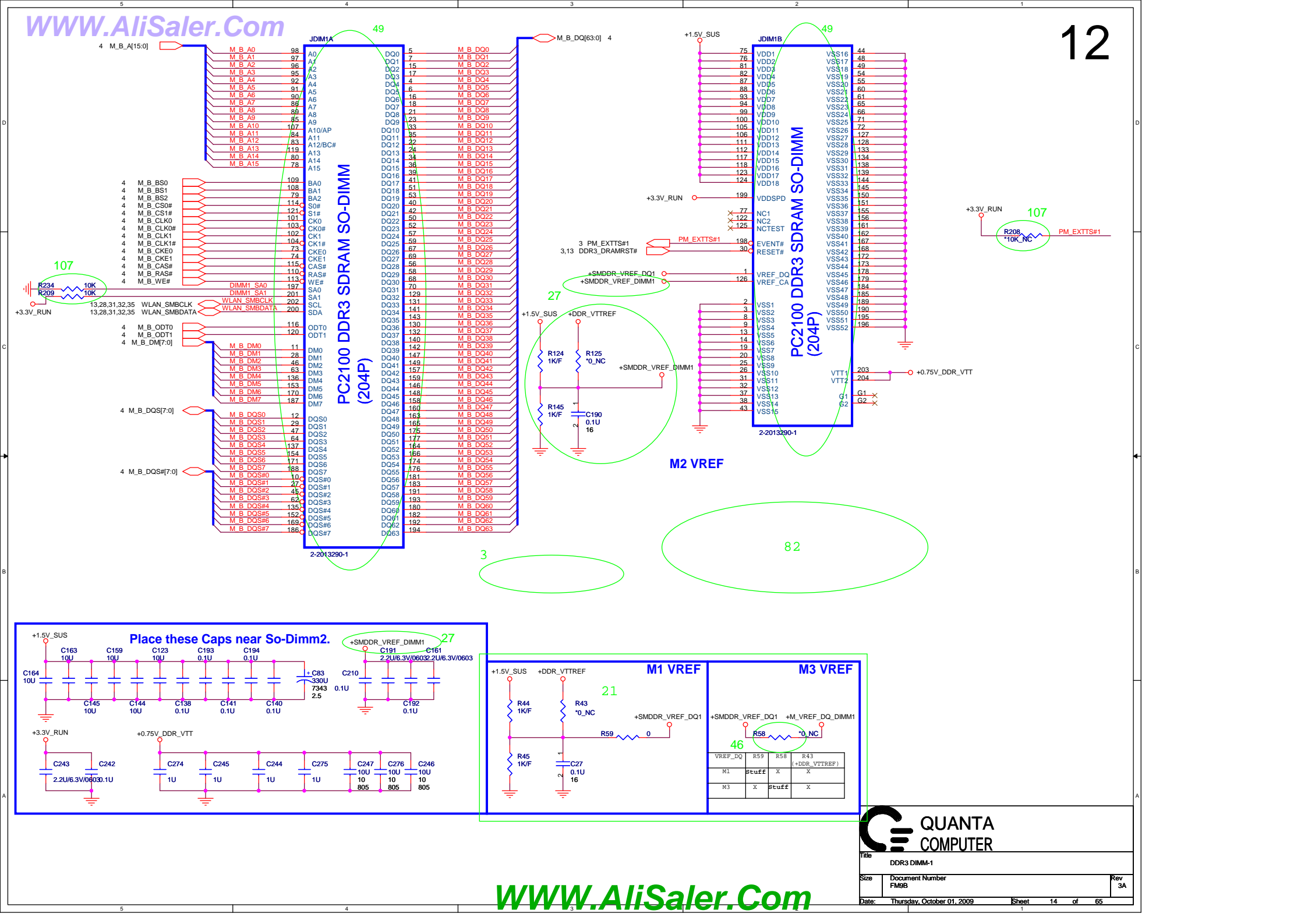
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IBEX PEAK-M 5/6			
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IBEX PEAK-M (GND)

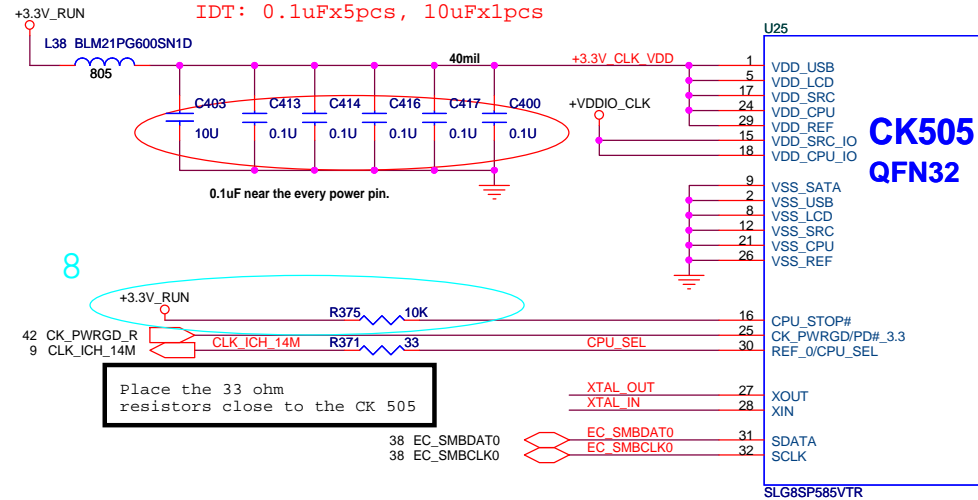


		
Title IBEX PEAK-M 6/6		
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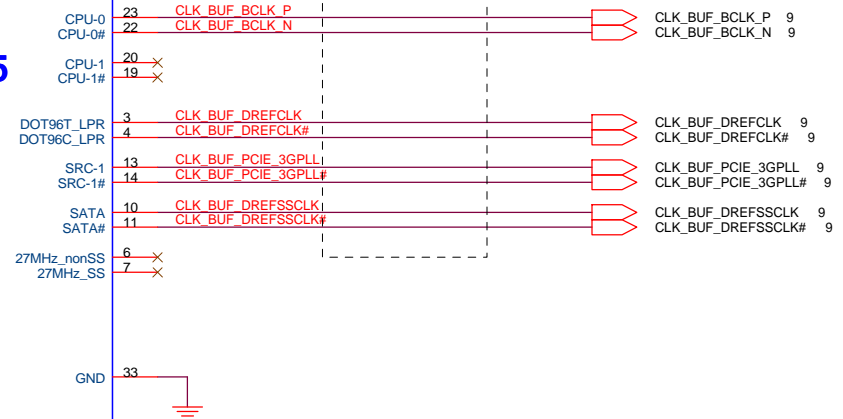




Realtek: 0.1uF x 6 pcs, 22uF x 1 pcs
IDT: 0.1uF x 5 pcs, 10uF x 1 pcs

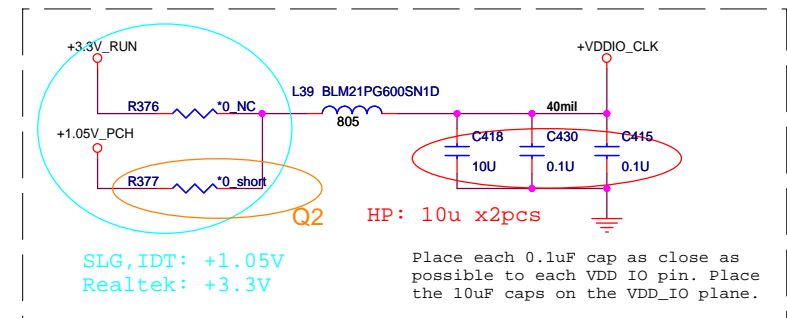
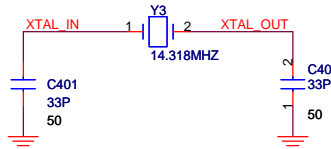


Place within 0.5" of CLKGEN

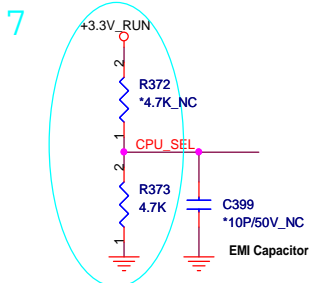


Realtek: 0.1uF x 3 pcs, 22uF x 1 pcs
IDT: 0.1uF x 2 pcs, 10uF x 1 pcs

Add capacitor pads for improving WWAN.




+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.




PIN	30	CPU_0	CPU_1
0 (default)		133MHz	133MHz
1 (0.7V-1.5V)		100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet (V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet (V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

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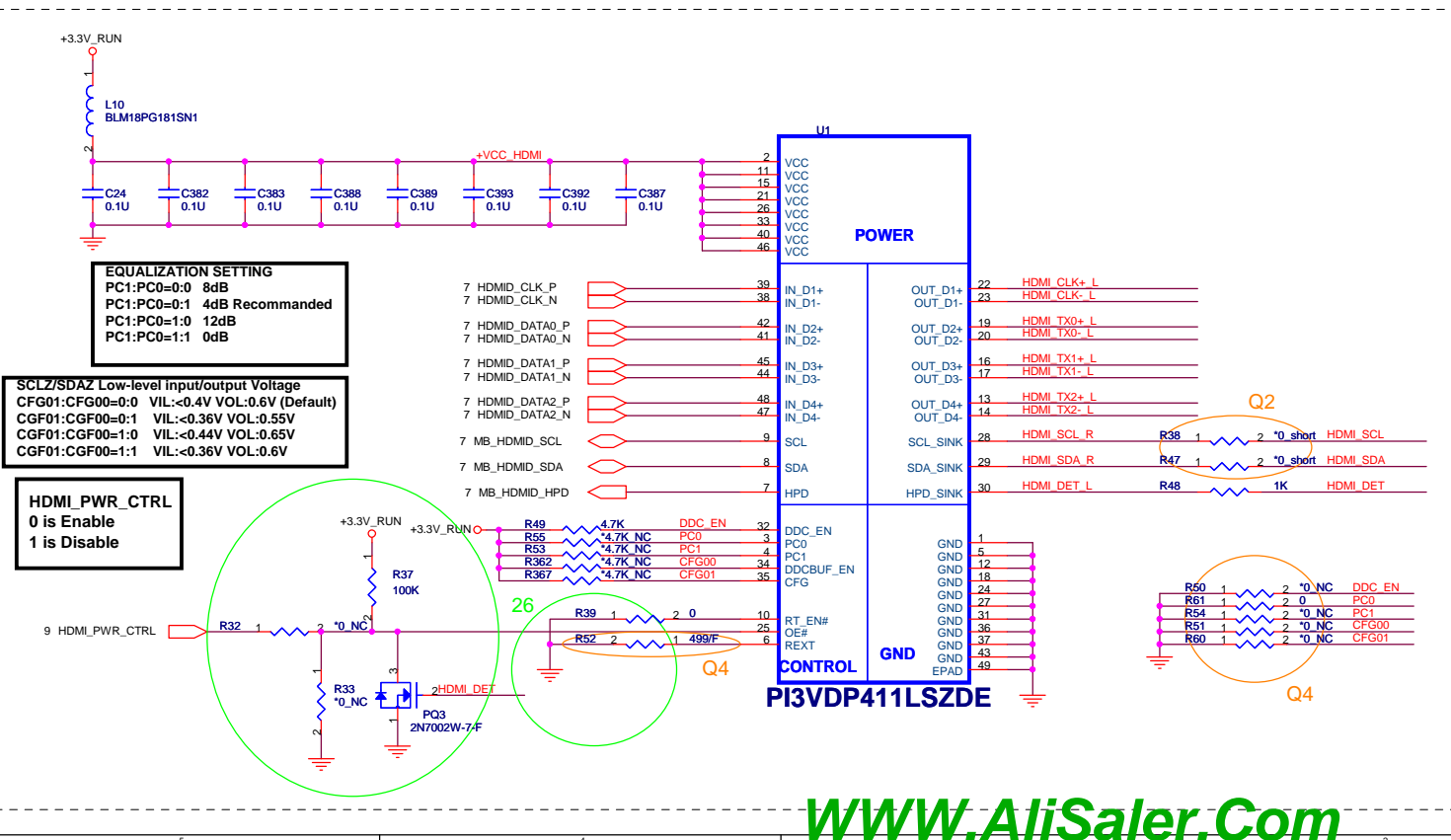
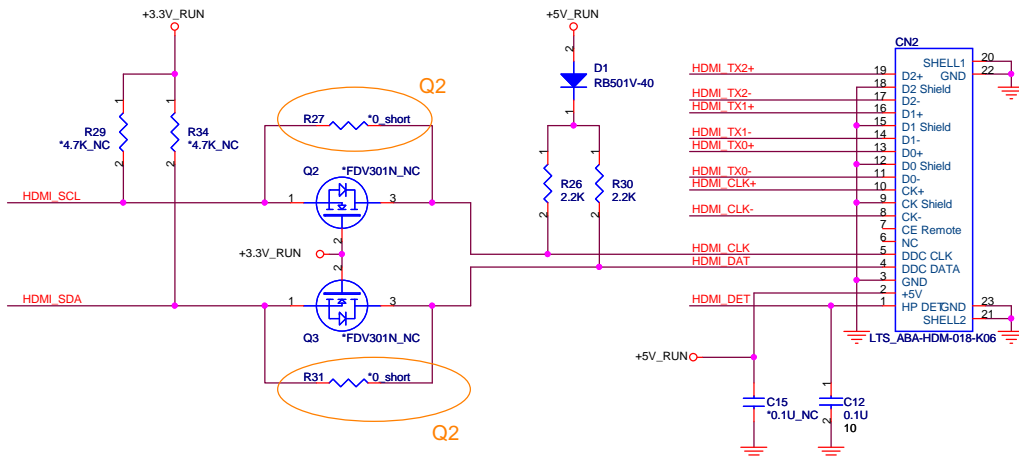
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Reserve for EMI and close to HDMI CONN

HDMI_CLK+_L	R7	300	HDMI_CLK_C	C16	0.1U	HDMI_CLK-_L
HDMI_TX0+_L	R8	300	HDMI_TX0_C	C19	0.1U	HDMI_TX0-_L
HDMI_TX1+_L	R15	300	HDMI_TX1_C	C20	0.1U	HDMI_TX1-_L
HDMI_TX2+_L	R16	300	HDMI_TX2_C	C22	0.1U	HDMI_TX2-_L

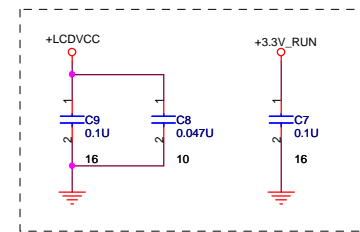
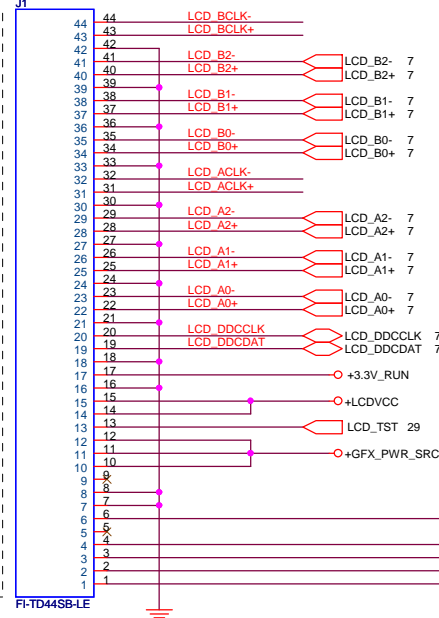
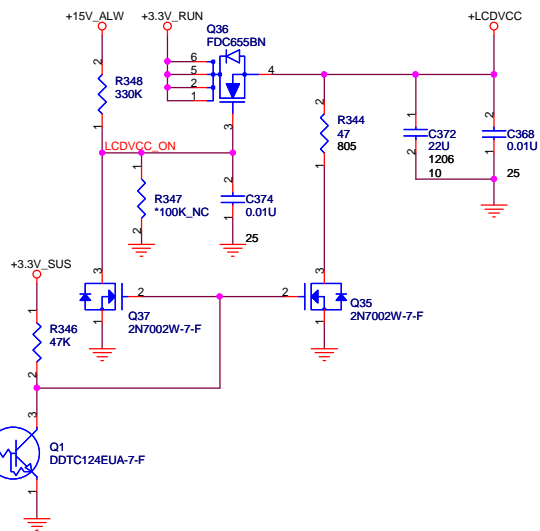
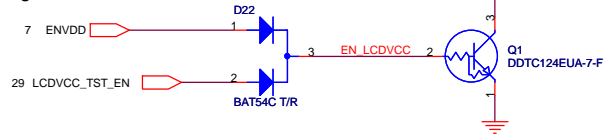


HDMI

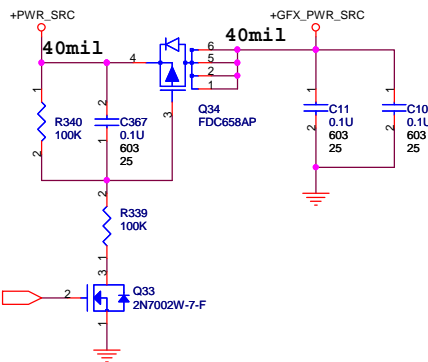
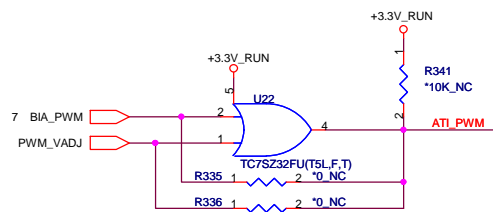


File	VGA-M82-S (PCIe)
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Support the new imbedded diagnostics.

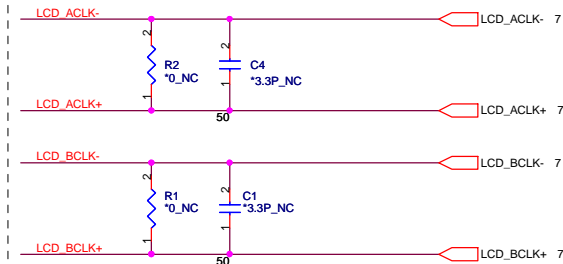


Address : A9H --Contrast
AAH --Backlight



Shunt capacitors on LVDS for improving WWAN.

LCD_B0-	C13	1	2	*3.3P_NC	50	LCD_B0+
LCD_B1-	C3	1	2	*3.3P_NC	50	LCD_B1+
LCD_B2-	C2	1	2	*3.3P_NC	50	LCD_B2+
LCD_A0-	C6	1	2	*3.3P_NC	50	LCD_A0+
LCD_A1-	C5	1	2	*3.3P_NC	50	LCD_A1+
LCD_A2-	C14	1	2	*3.3P_NC	50	LCD_A2+

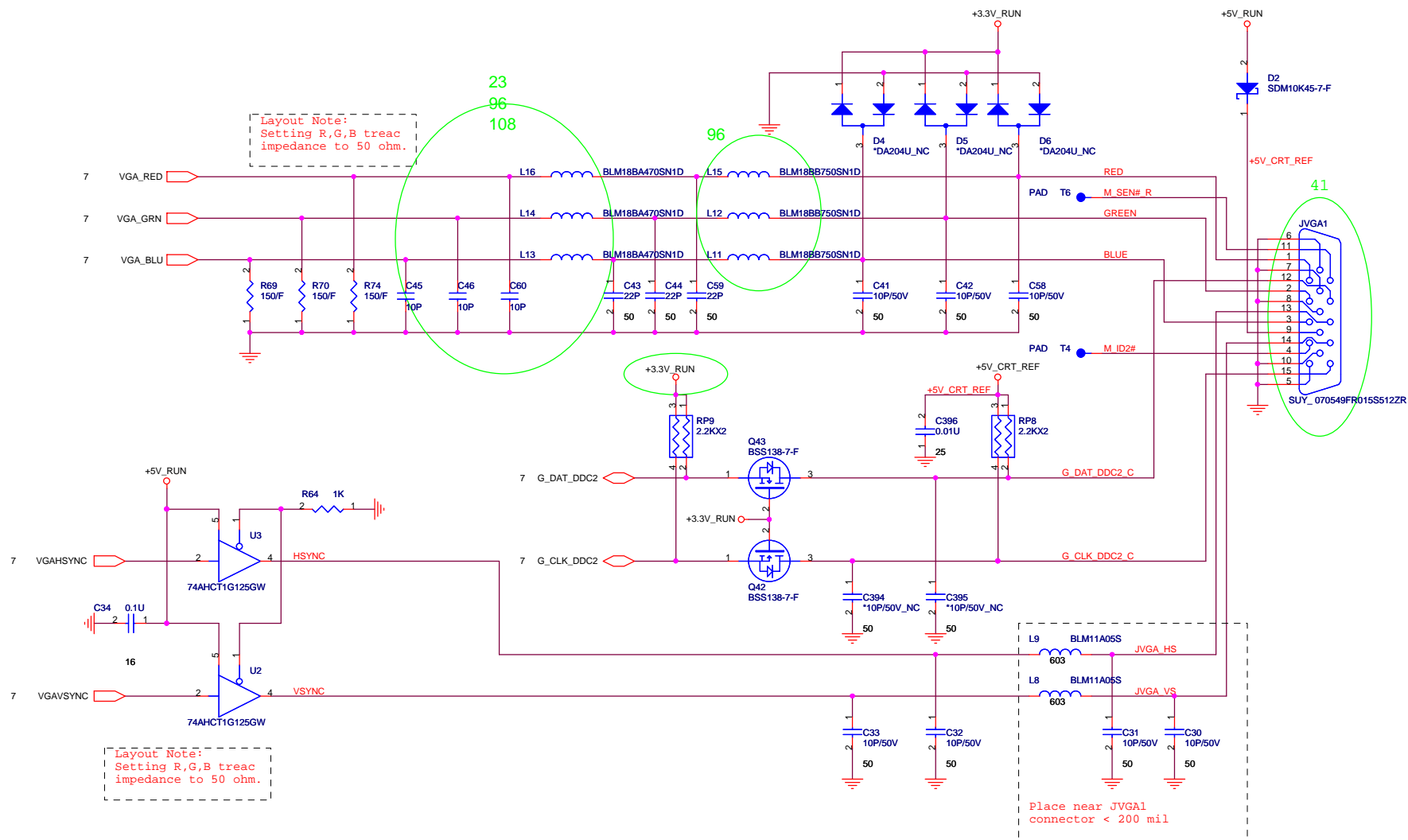


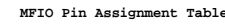
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Title: LCD CONN & CK-SSCD

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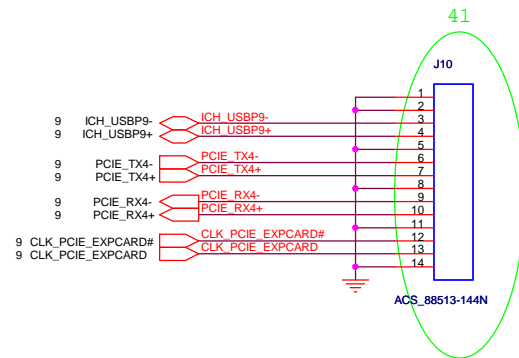
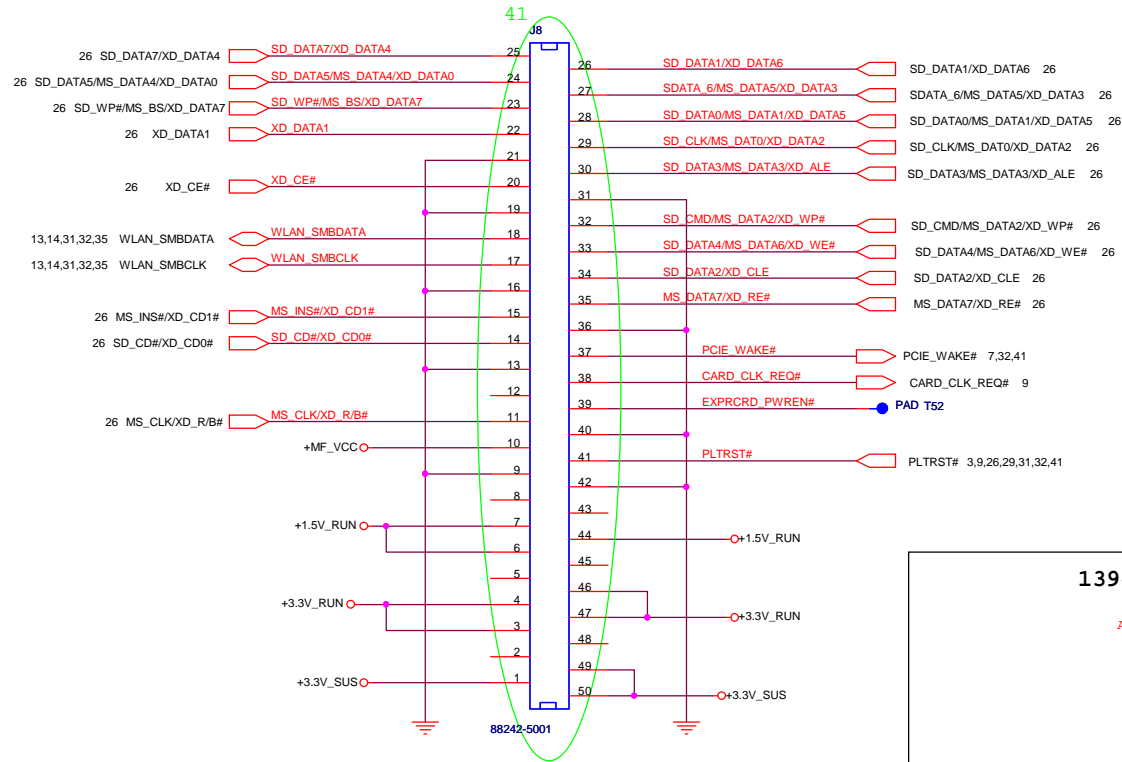




MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	-	D6
02	D0	D1	D5
03	D7	-	D4
04	D6	D5	D3
05	CLK	D0	D2
06	-	-	D1
07	D5	D4	D0
08	CMD	D2	WP#
09	D4	D6	WE#
10	D3	D3	ALE
11	D2	-	CLE
12	-	-	CE#
13	-	D7	RE#
14	-	CLK	R/B#

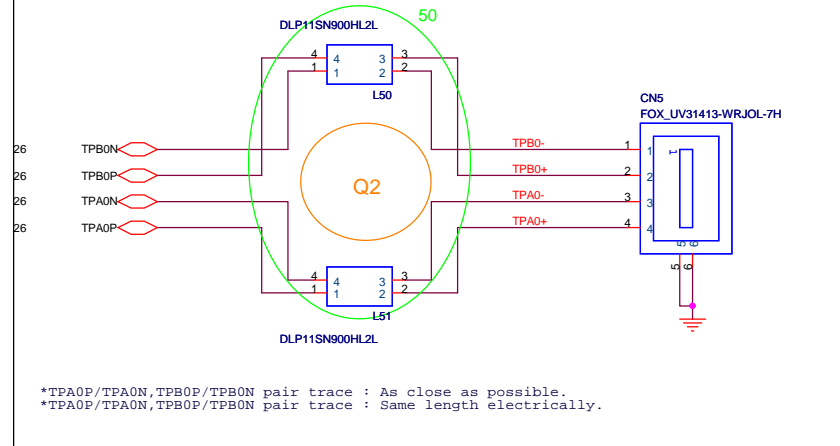
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Express Card/CARD READER

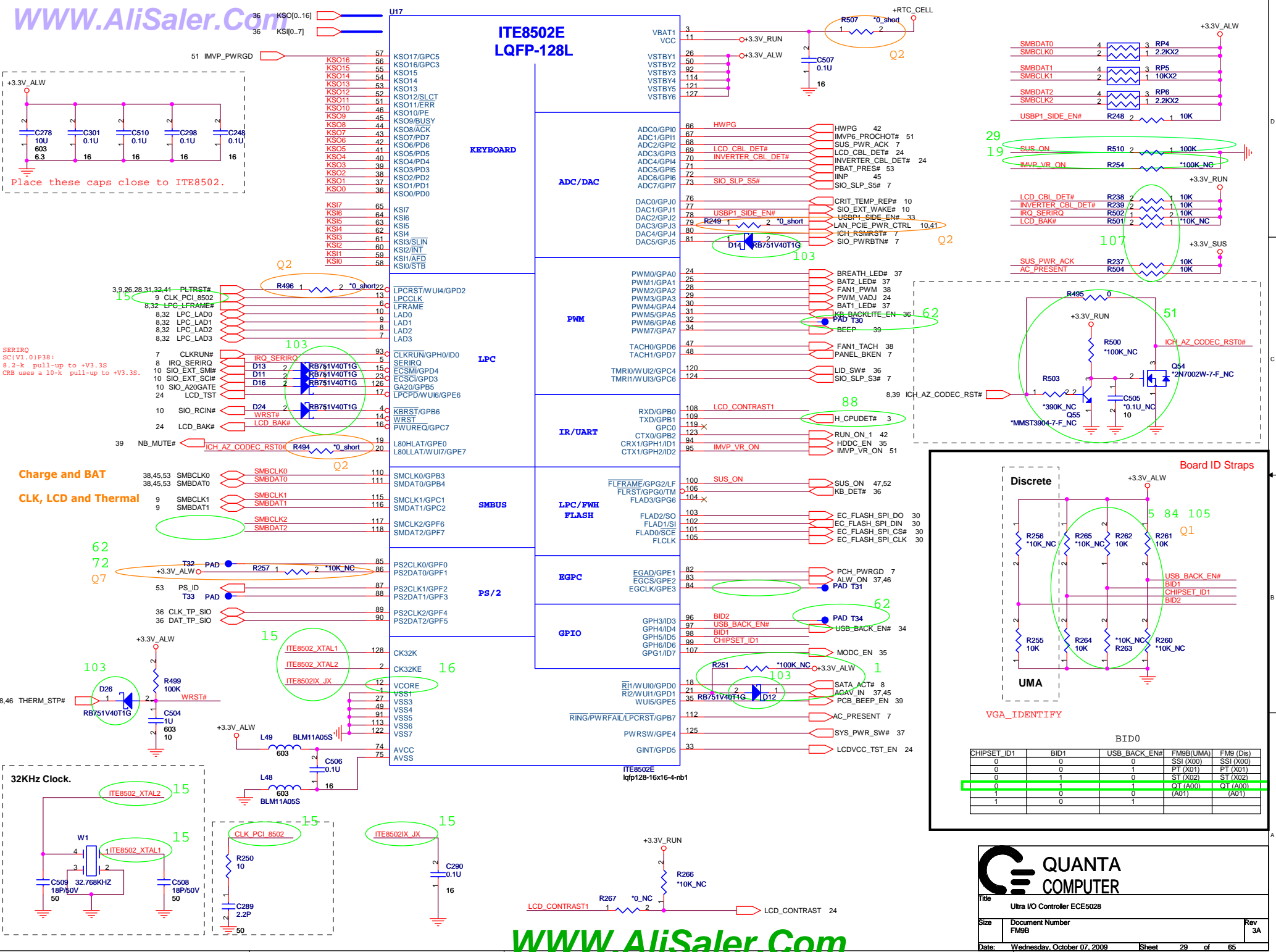


1394 CONNECTOR

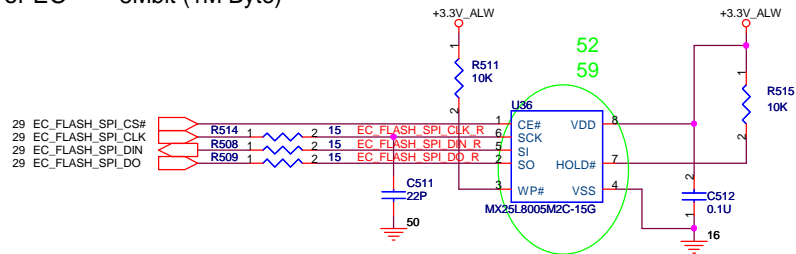
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.



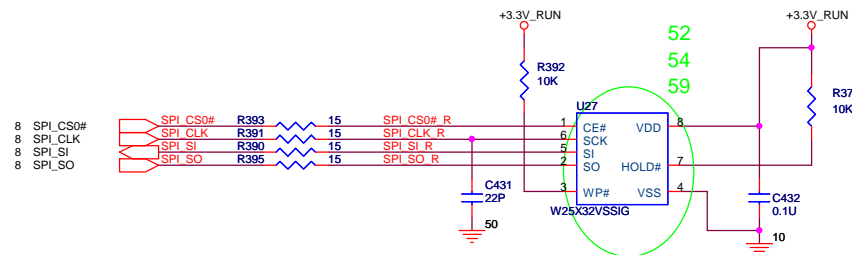
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ExpressCard/SmartCard		
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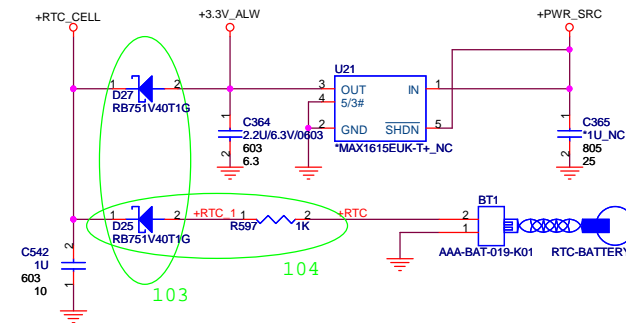
For EC 8Mbit (1M Byte)



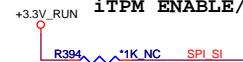
For PCH 32Mbit (4M Byte)



RTC BATTERY



iTPM ENABLE/DISABLE



TPM Function	R712
Enable	Mount
Disable	NC (Default)



Ultra I/O Controller ECE5028

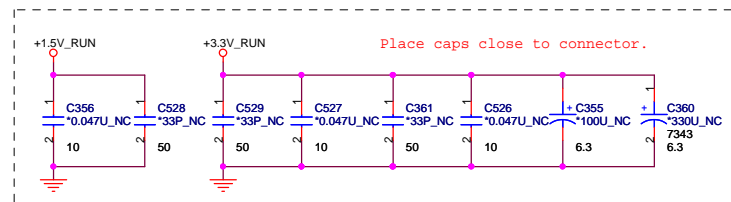
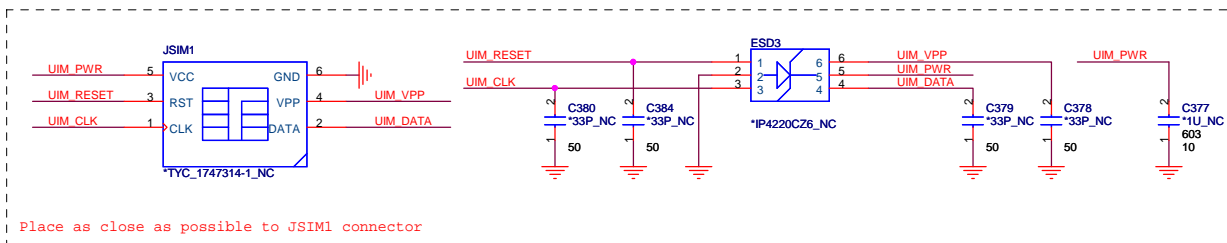
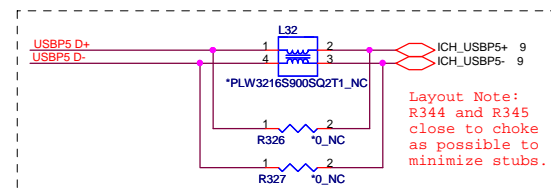
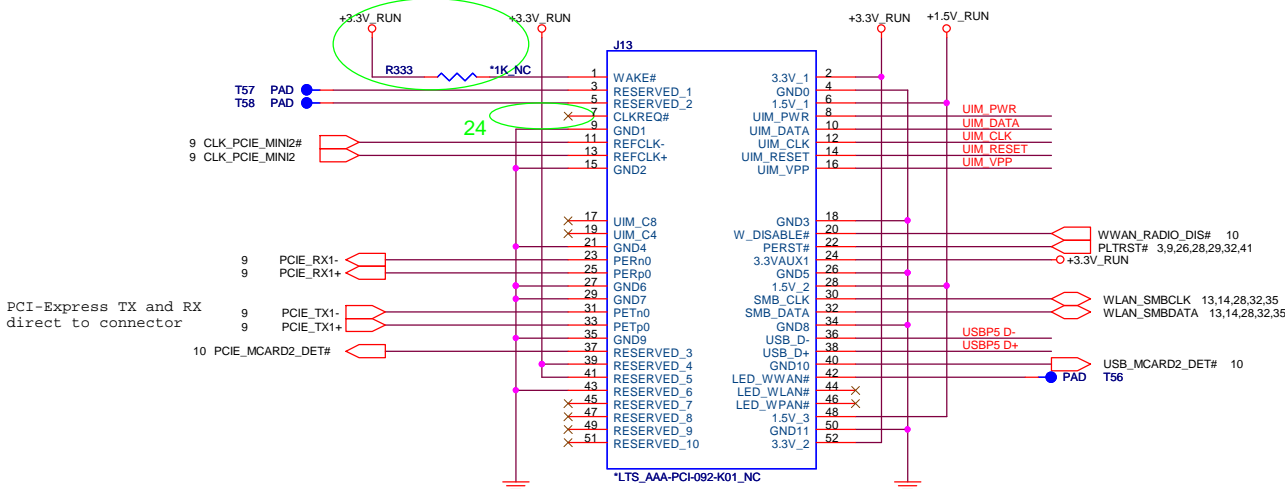
Size Document Number
FM9B

Rev
3A

Date: Thursday, October 01, 2009

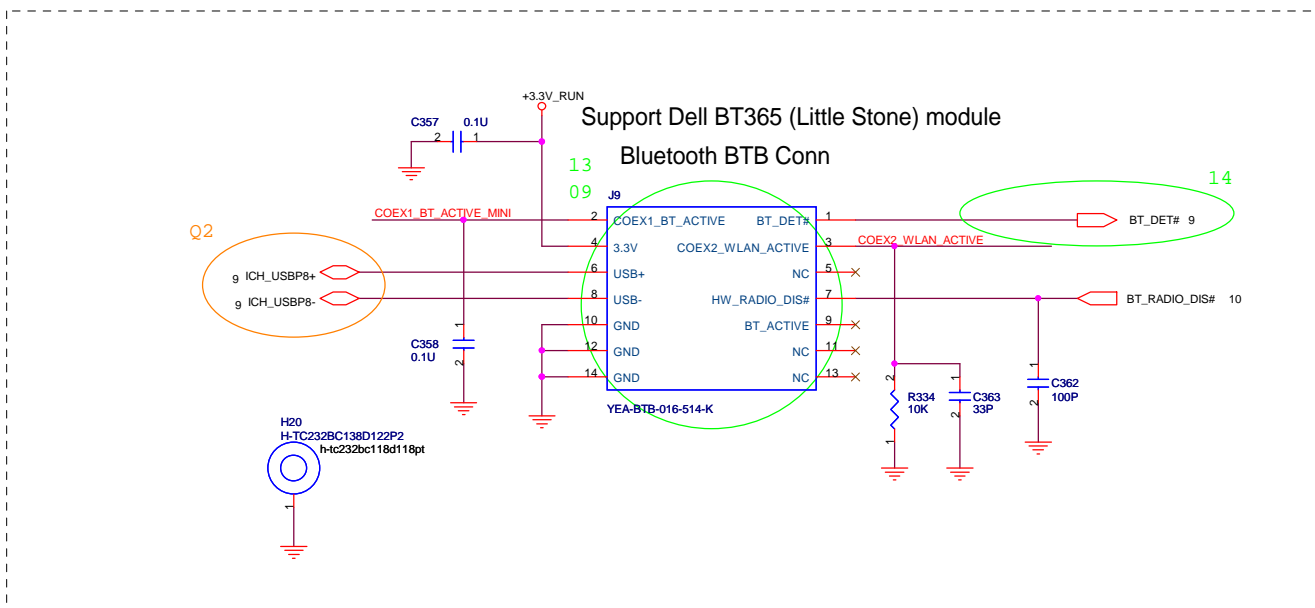
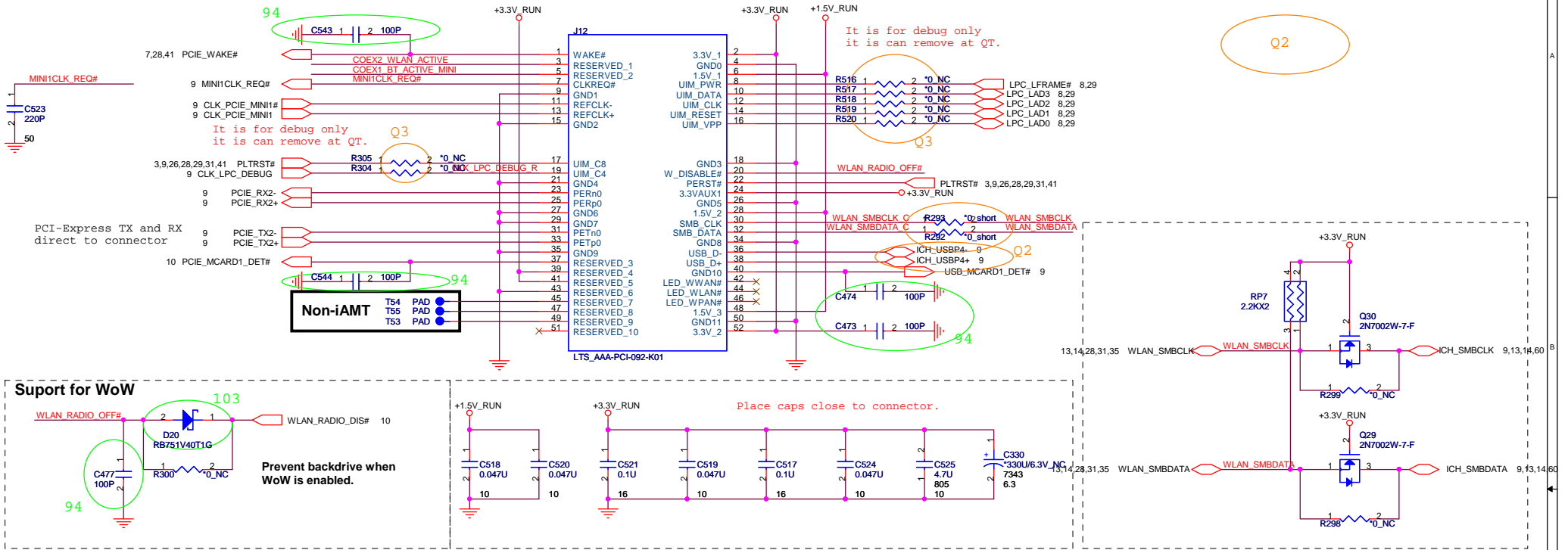
Sheet 30 of 65

MiniCard WWAN connector

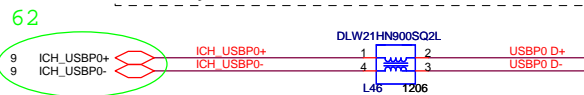


Title			MINI-PCI
Size	Document Number	Rev	
	FM9B	3A	
Date:	Thursday, October 01, 2009	Sheet	31 of 65

MiniCard WLAN connector



External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



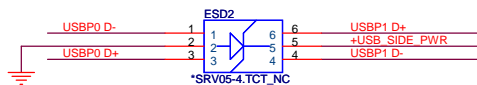
Q2



Q2

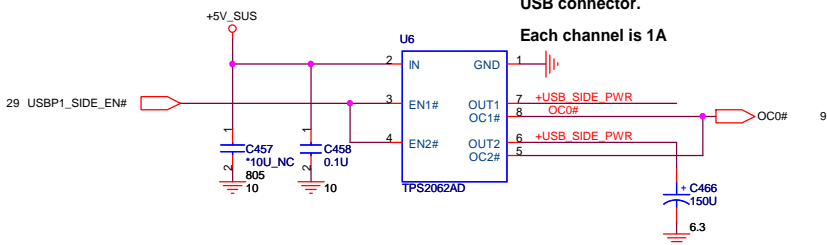
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.



Place one 150uF cap by each USB connector.

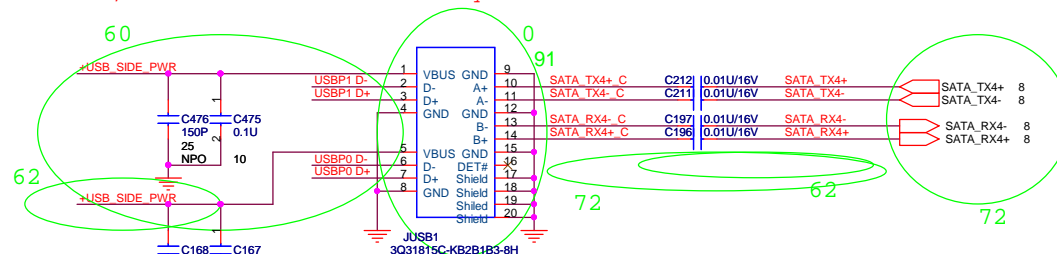
Each channel is 1A



62

Side External USBX2

PN is old, Because New Part can't ready before SST build.



Please put those on the same side of MB PCB

USBx2 & ESATA COMBO

USB BUS SW

62

E-SATA Re-driver

72

62



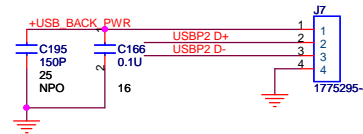
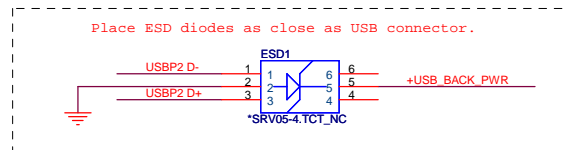
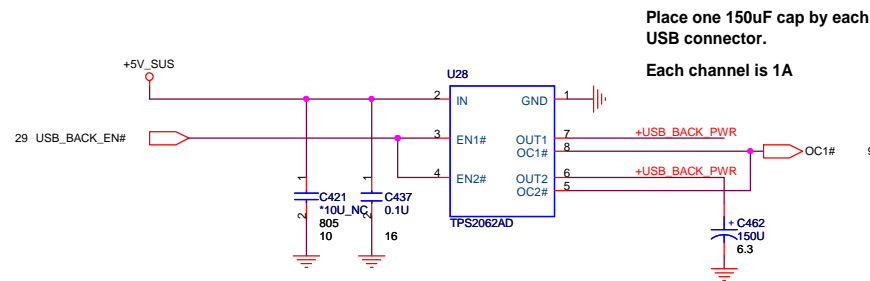
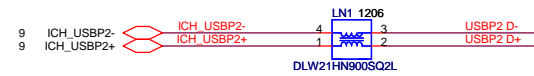
File SERIAL PORT & USB

Size Document Number FM9B

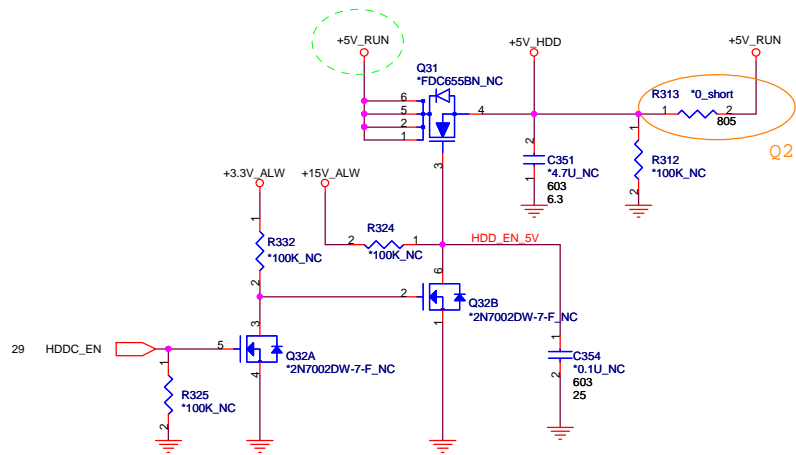
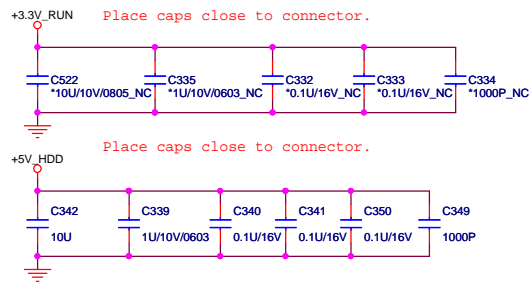
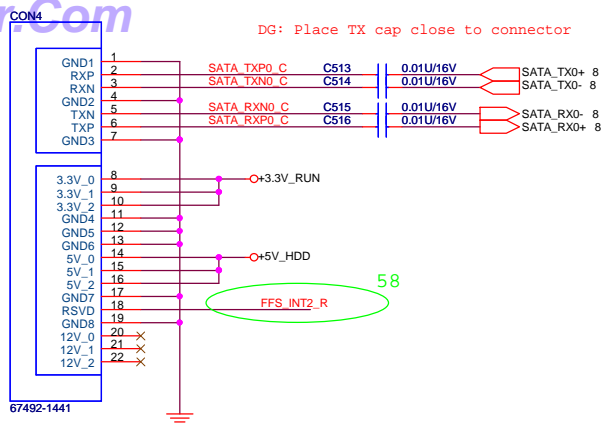
Date: Thursday, October 01, 2009

Rev 3A

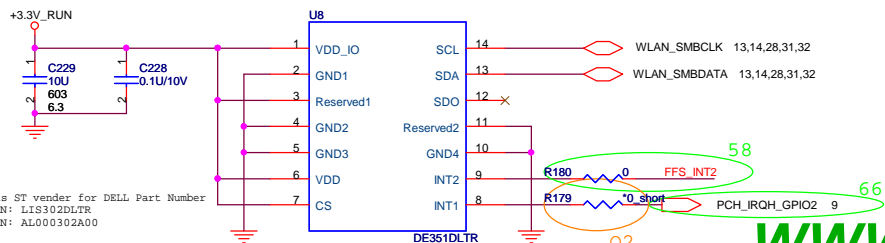
Sheet 33 of 65



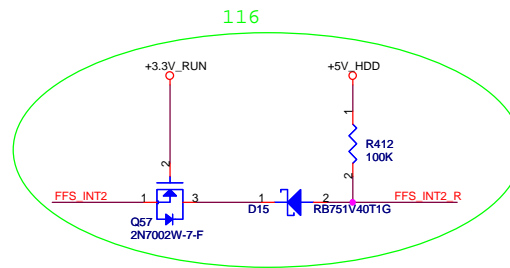
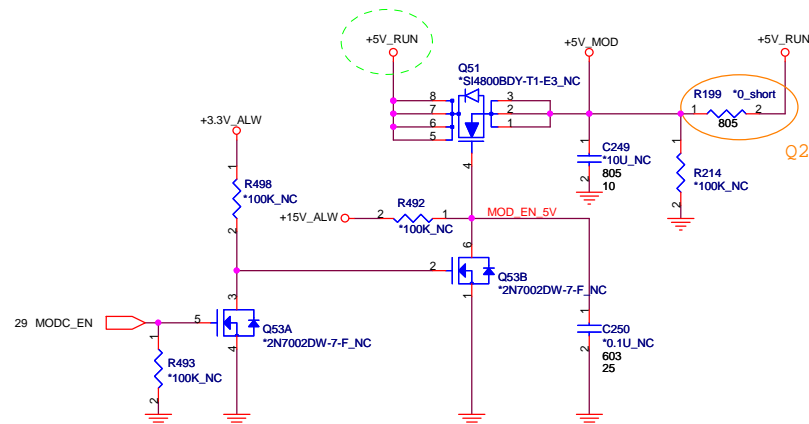
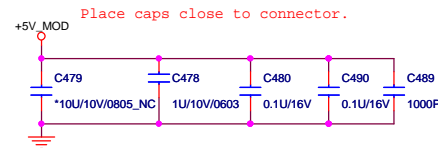
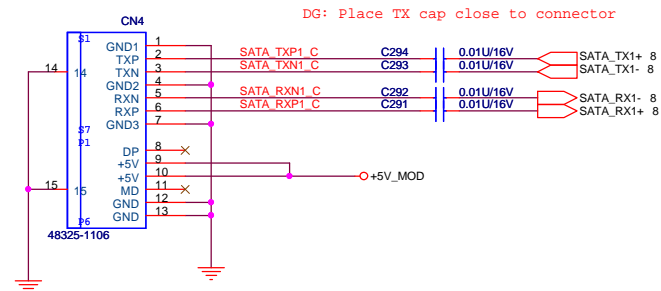
SATA Connector.



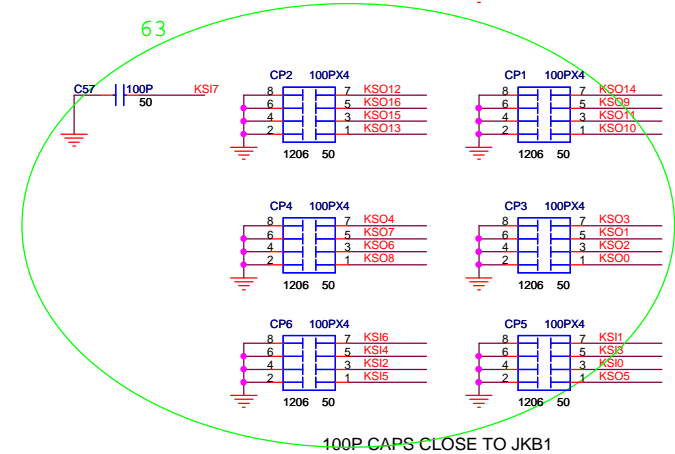
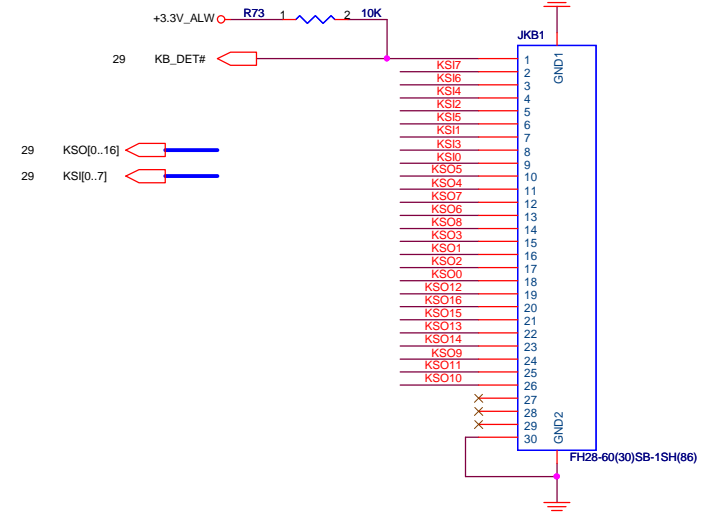
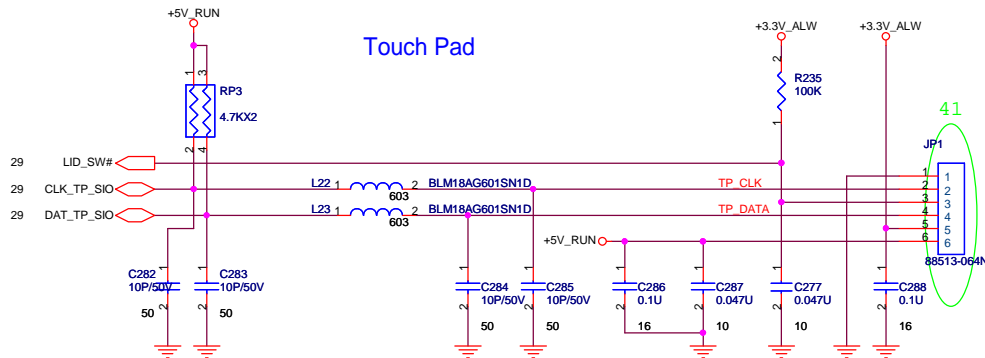
3-axis Fall Sensor (HDD data protector)



ODD Connector

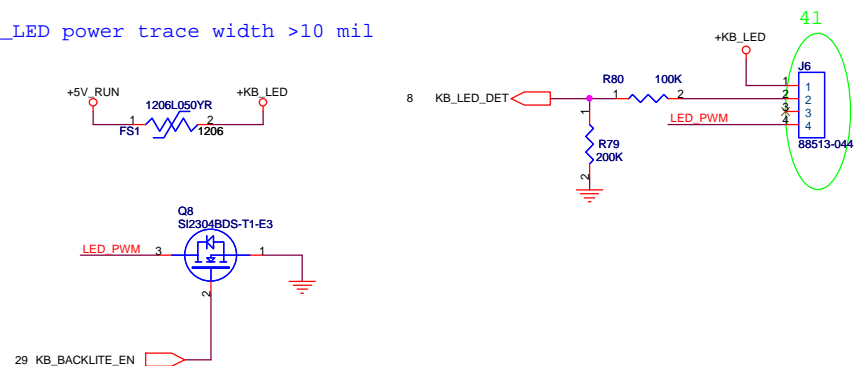


Title				SATA (HDD&CD_ROM)			
Size		Document Number				Rev	
		FM9B				3A	
Date:		Monday, October 05, 2009		Sheet		35 of 65	



Key board illumination

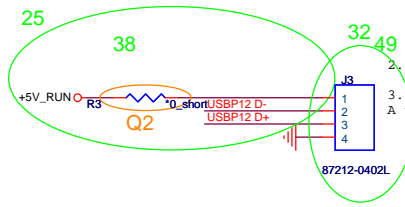
+KB_LED power trace width >10 mil



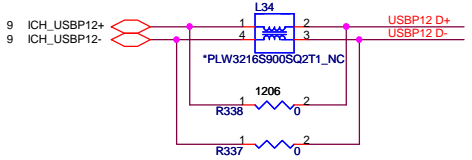
Title TOUCH PAD, BULE TOOTH & FIR		
Size	Document Number FM9B	Rev 3A
Date: Thursday, October 01, 2009	Sheet 36	of 65

Touch Screen Module

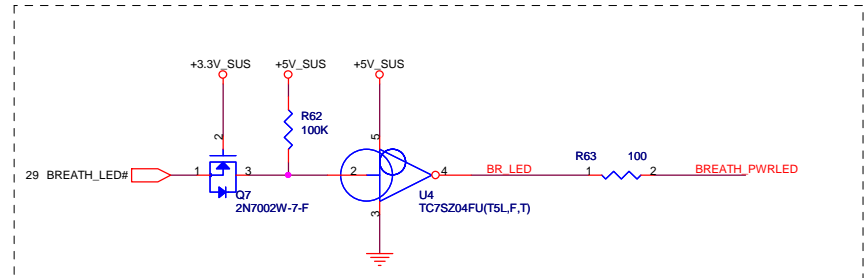
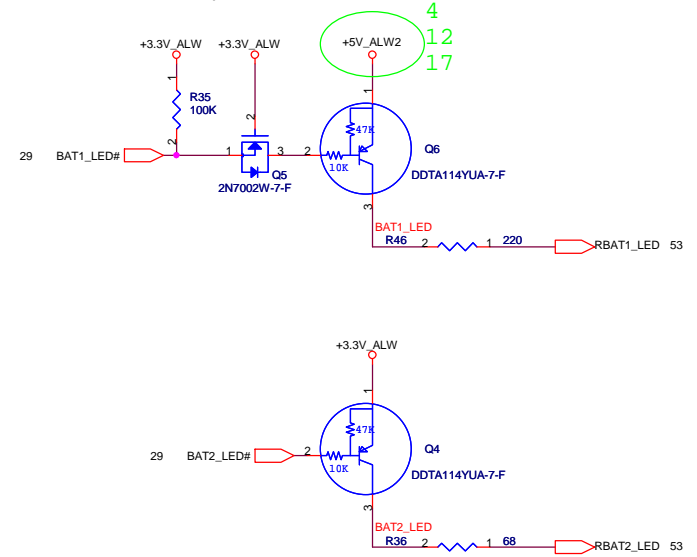
- Note:
1. VBUS IND:VBUS indication should be supplied to single the DuoSense to connect According to the USB 2.0 specification. A GND voltage from the host should indicate a connection.
 2. Maximum cable resistance on VCC, GND should be 150m ohm.
 3. FPC cable should support 12MHz USB singles. A tri-state should indicate no connection.



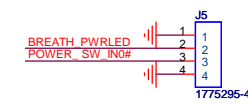
Need check the connector footprint and symbol.



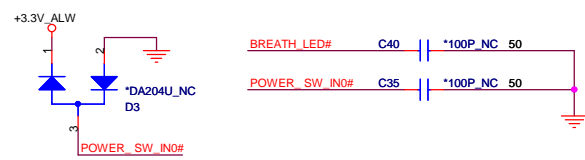
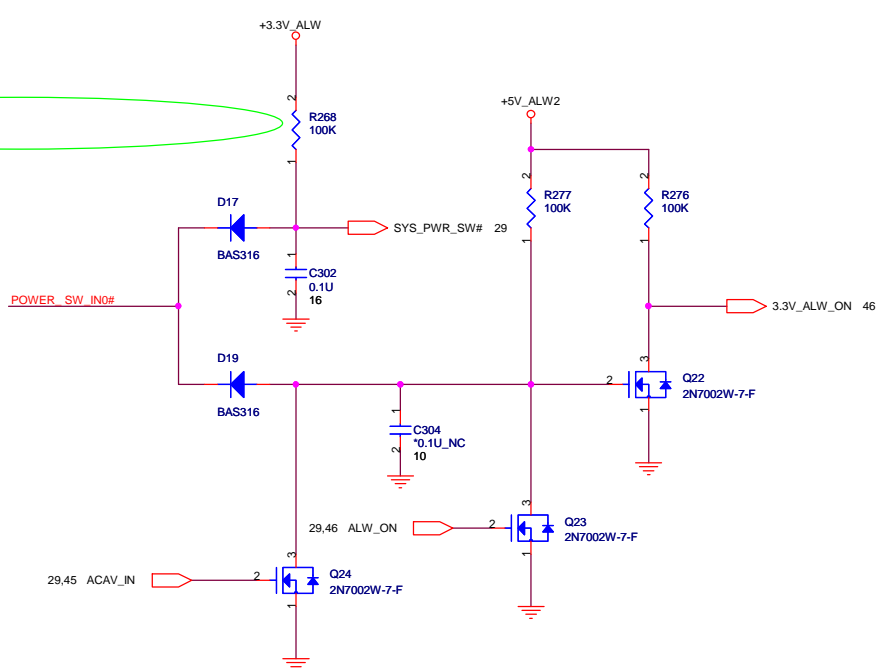
Battery status.



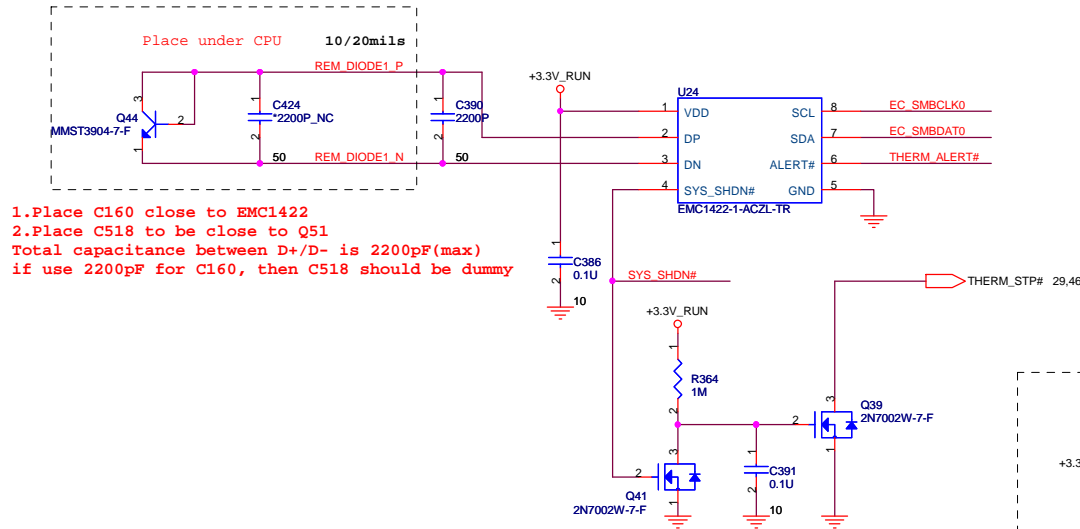
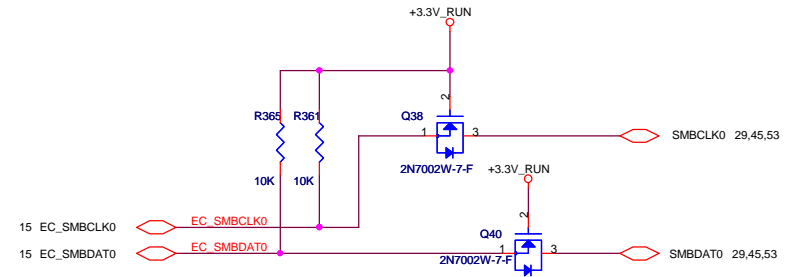
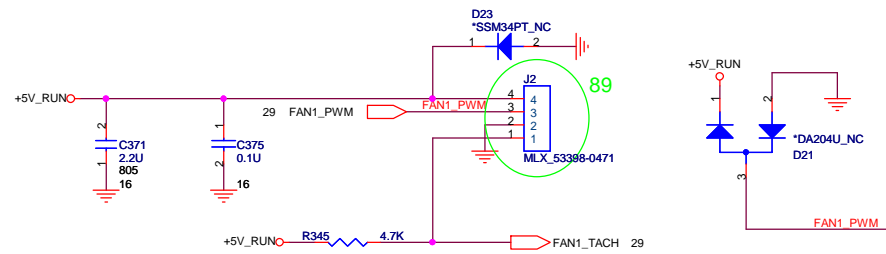
Power button Cable



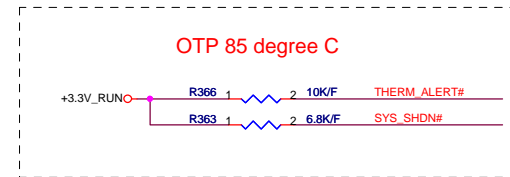
3VALW ON POWER LOGIC

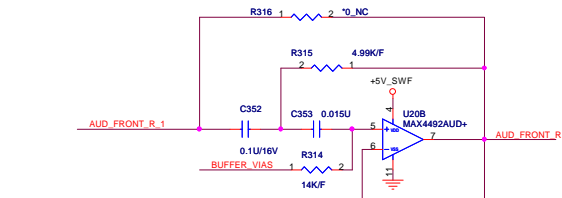
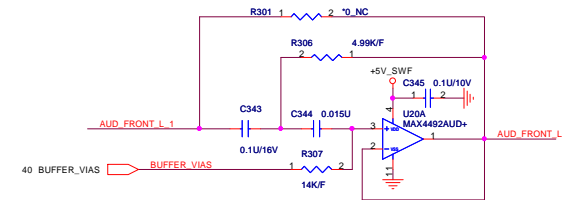


Title		
SWITCH, KEYBOARD & LED&Touch Screen Module		
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Date:	Monday, October 05, 2009	Sheet 37 of 65

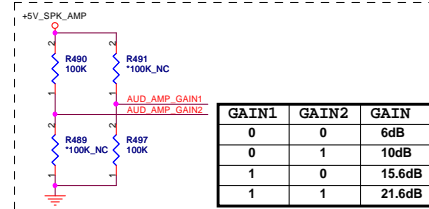
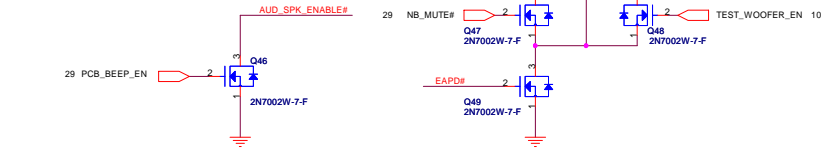


1.Place C160 close to EMC1422
2.Place C518 to be close to Q51
Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C160, then C518 should be dummy

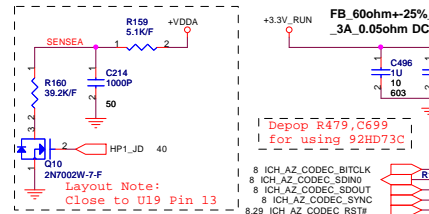
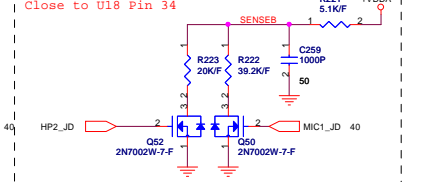
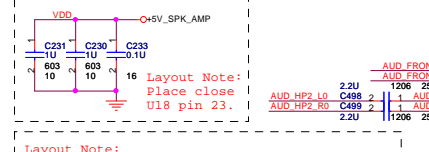




EAPD#	NB_MUTE#	TEST_WOOFER_EN	AUD_SPK_ENABLE#	SUB_MUTE#
0	0	0	H	L
0	0	1	H	L
0	1	0	H	L
0	1	1	H	L
1	0	0	H	L
1	0	1	H (Disable SPK)	H (Test Woofers)
1	1	0	L (Test SPK)	L (Disable Woofers)
1	1	1	L	H



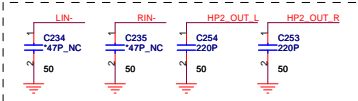
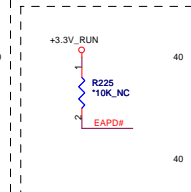
GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



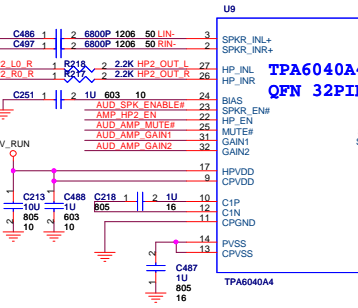
Depop R479,C699 for using 92HD73C

ICH_AZ_CODEC_BITCLK R182 22K NC C239 1P NC

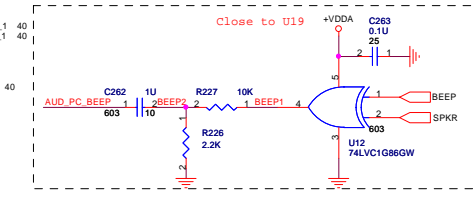
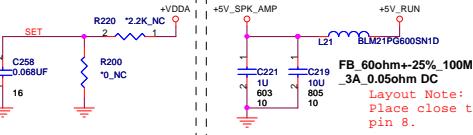
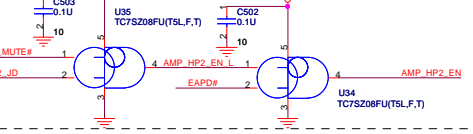
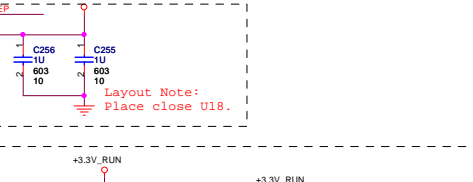
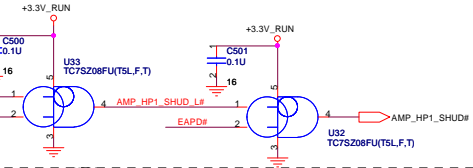
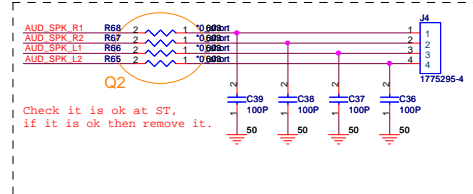
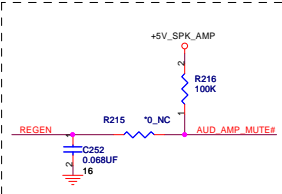
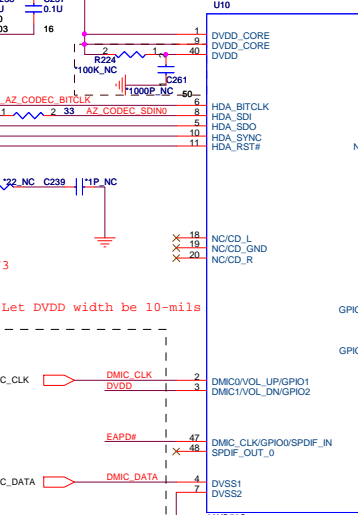
Depop R477,R478,R484,R473 Pop R476,R480,R483,R475 for using 92HD73C R476,R483 close to U19, Let DVDD width be 10-mils



INTERNAL SPEAKER AMP



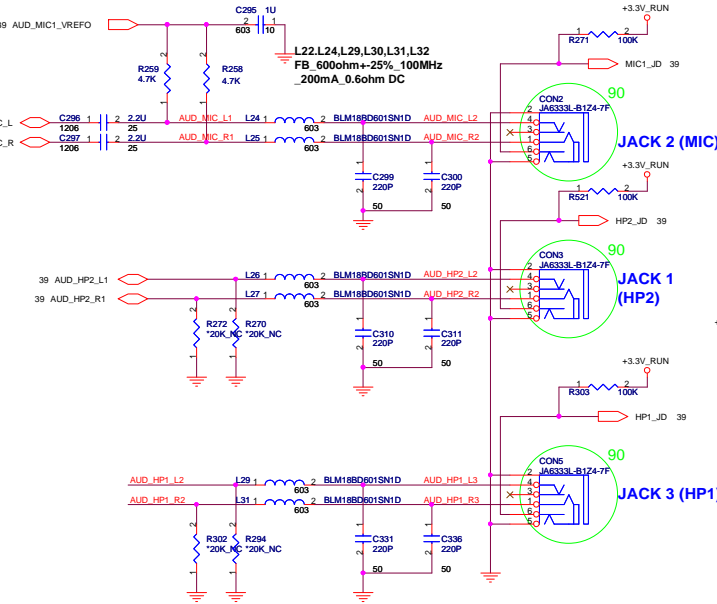
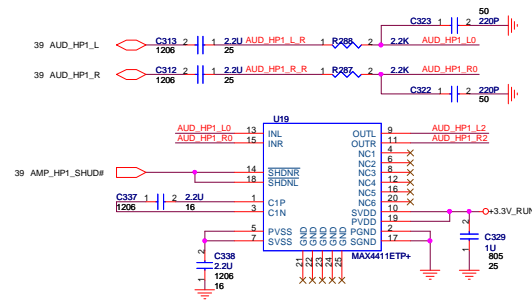
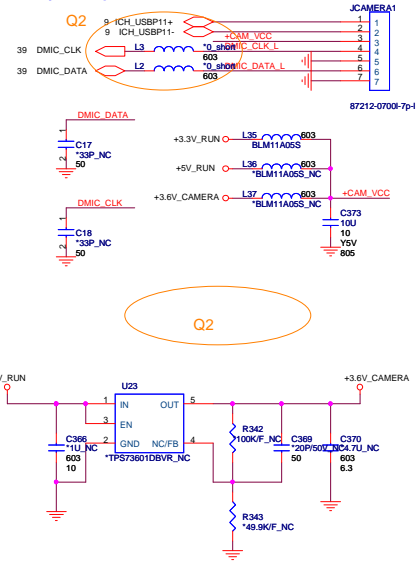
AZALIA (HD) CODEC



QUANTA COMPUTER

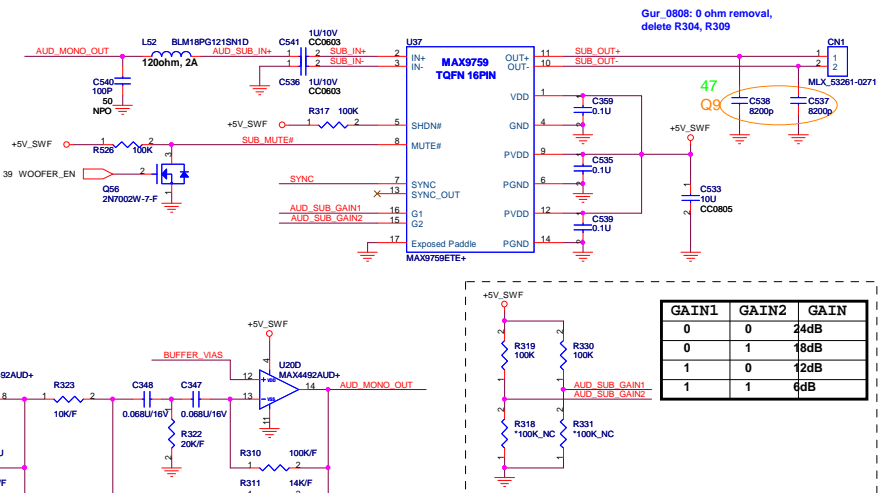
File	Azalia CODEC	Rev	3A
Size	Document Number FM98		
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Headphone Jack
Stereo MIC Jack

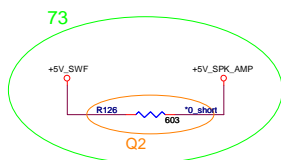


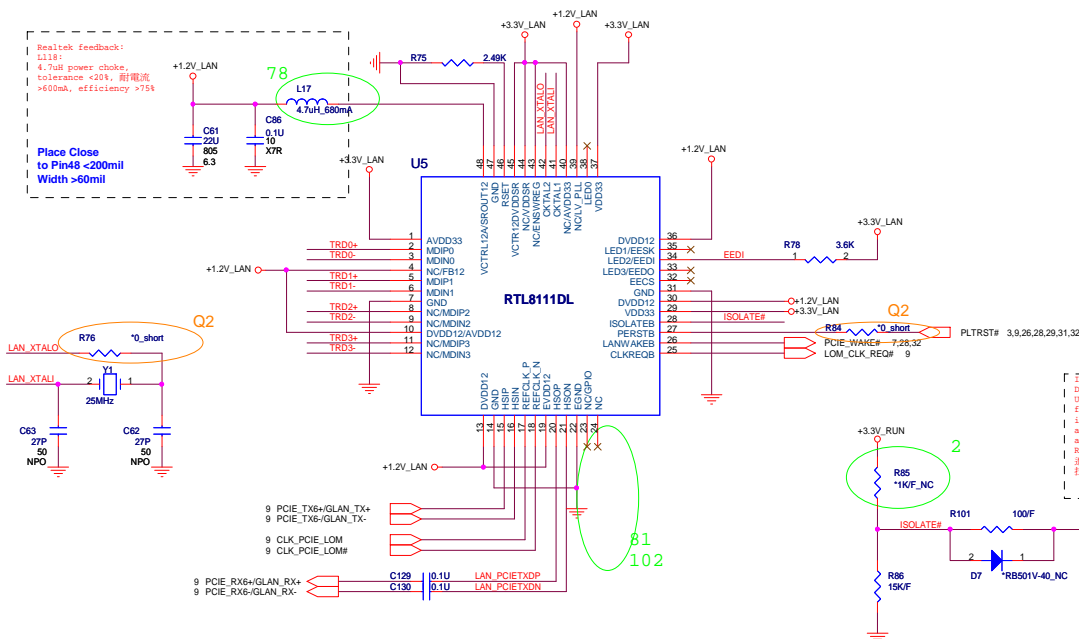
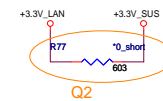
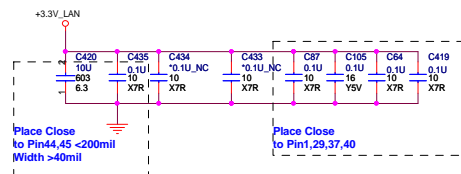
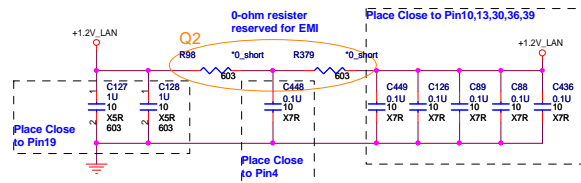
INTERNAL SUBWOOFER AMP

SYNC	Condition
VDD	Spread-spectrum mode with $f_S = 1200\text{kHz} \pm 70\text{kHz}$.
GND	Fixed-frequency mode with $f_S = 1100\text{kHz}$.
FLOAT	Fixed-frequency mode with $f_S = 1500\text{kHz}$.
Clocked	Fixed-frequency mode with $f_S = \text{external clock frequency}$.

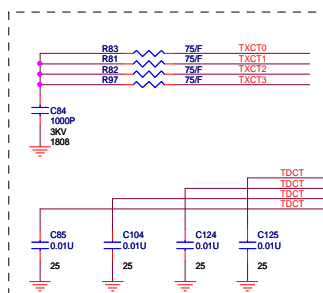
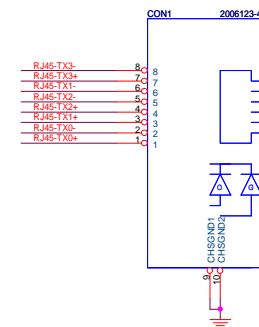


GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

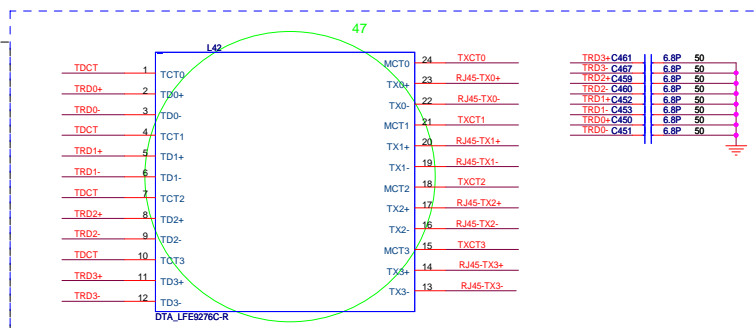


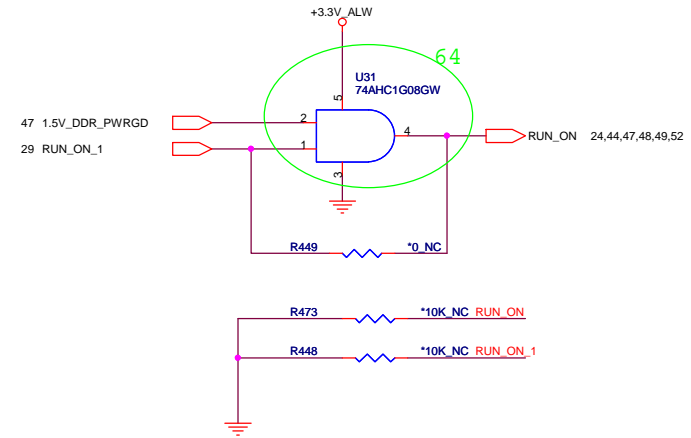
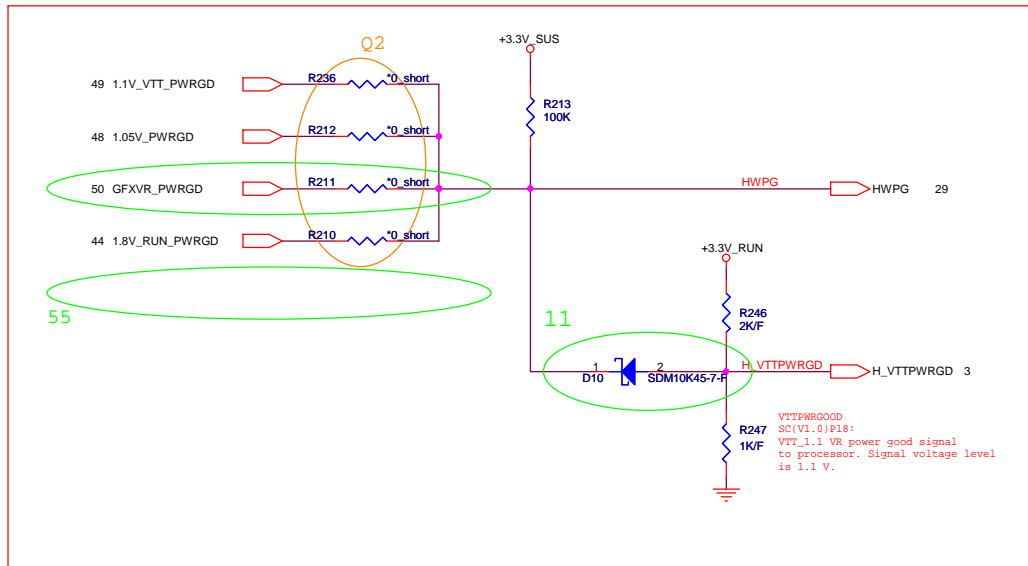
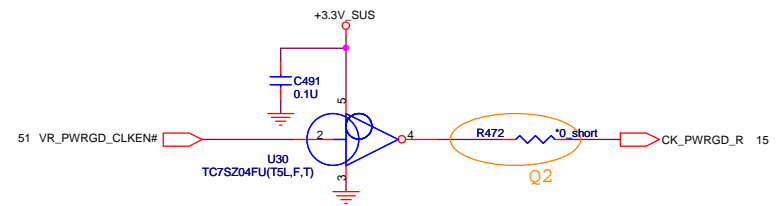



RJ-45 Connector

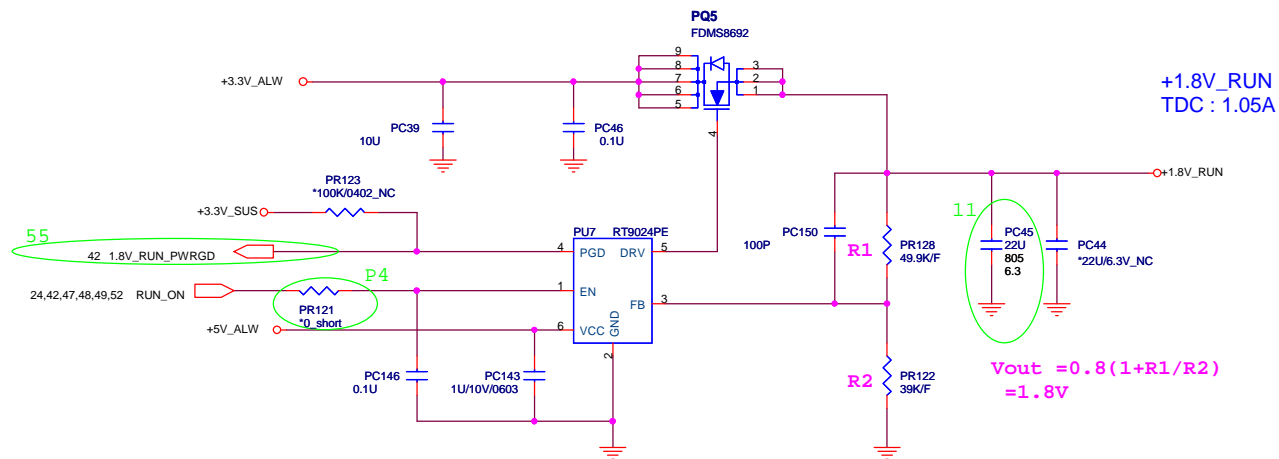


LAYOUT NOTE:
CAP CLOSE TO TRANSFORMER
one cap for each pin
Reserved for EMI.



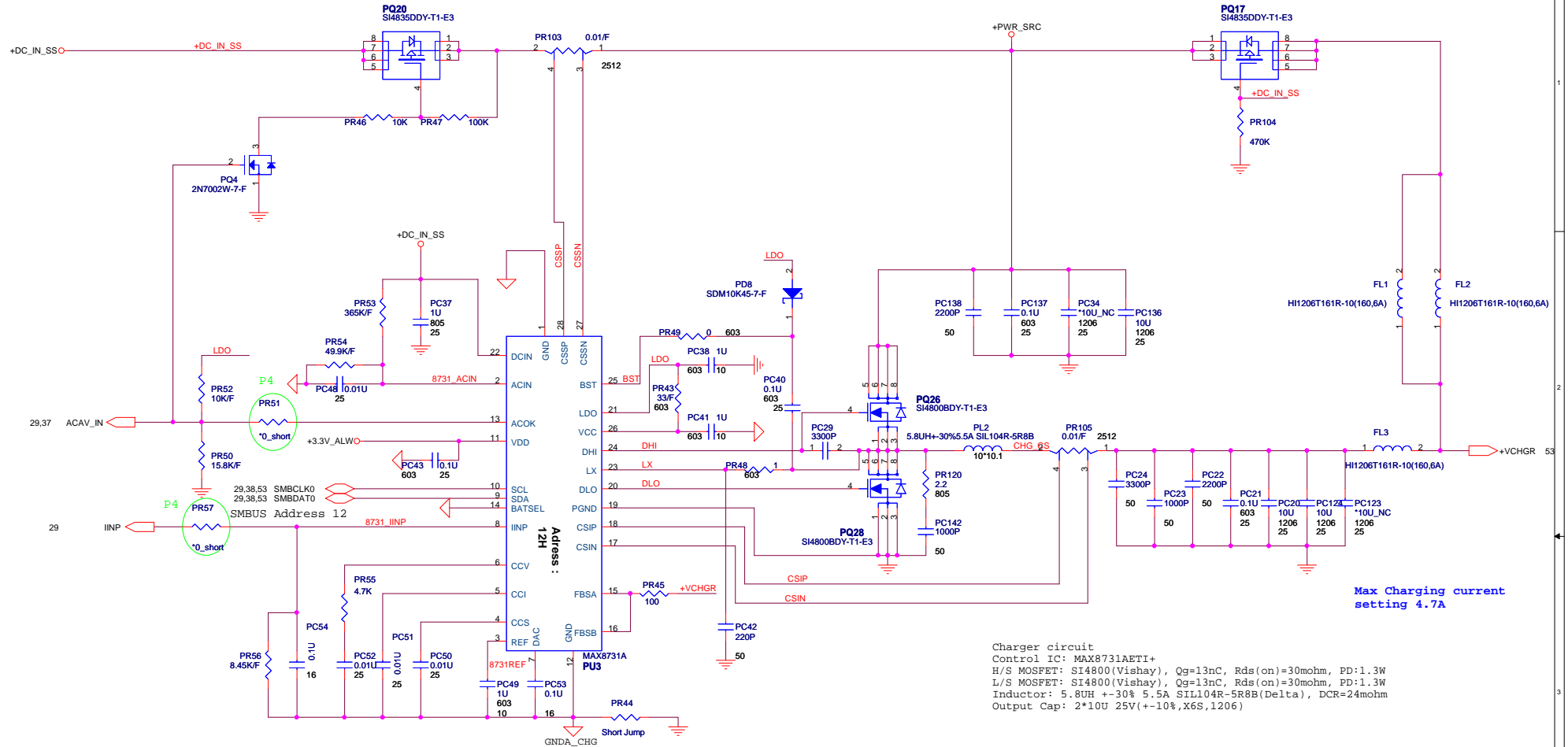


 QUANTA COMPUTER		
Title Battery Selector		
Size	Document Number FM9B	Rev 3A
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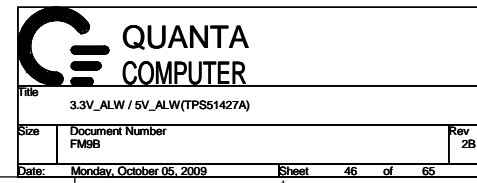
Continuous current : 13A
Rds(on) : 18mohm

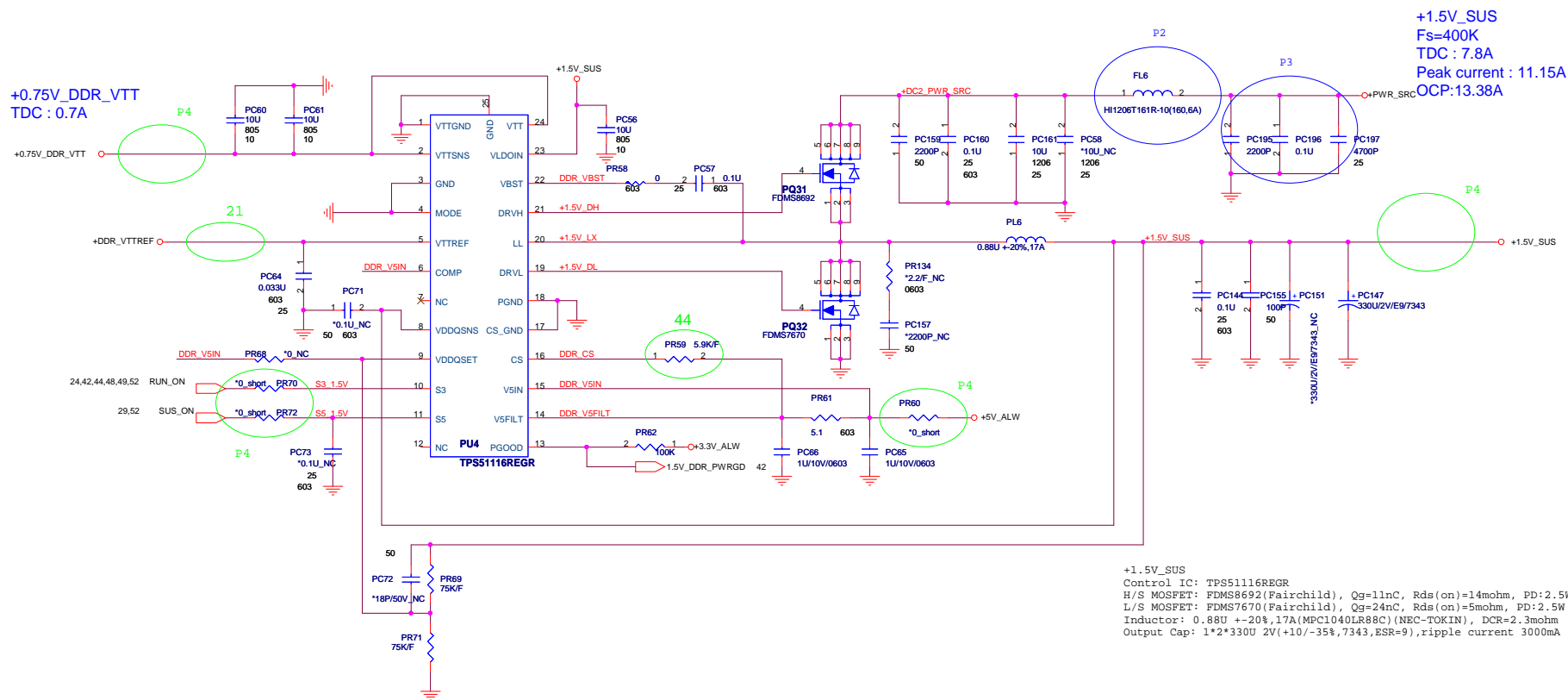
Continuous current : 13A
Rds(on) : 18mohm



QUANTA
COMPUTER

Title			Charger (MAX8731)
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VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

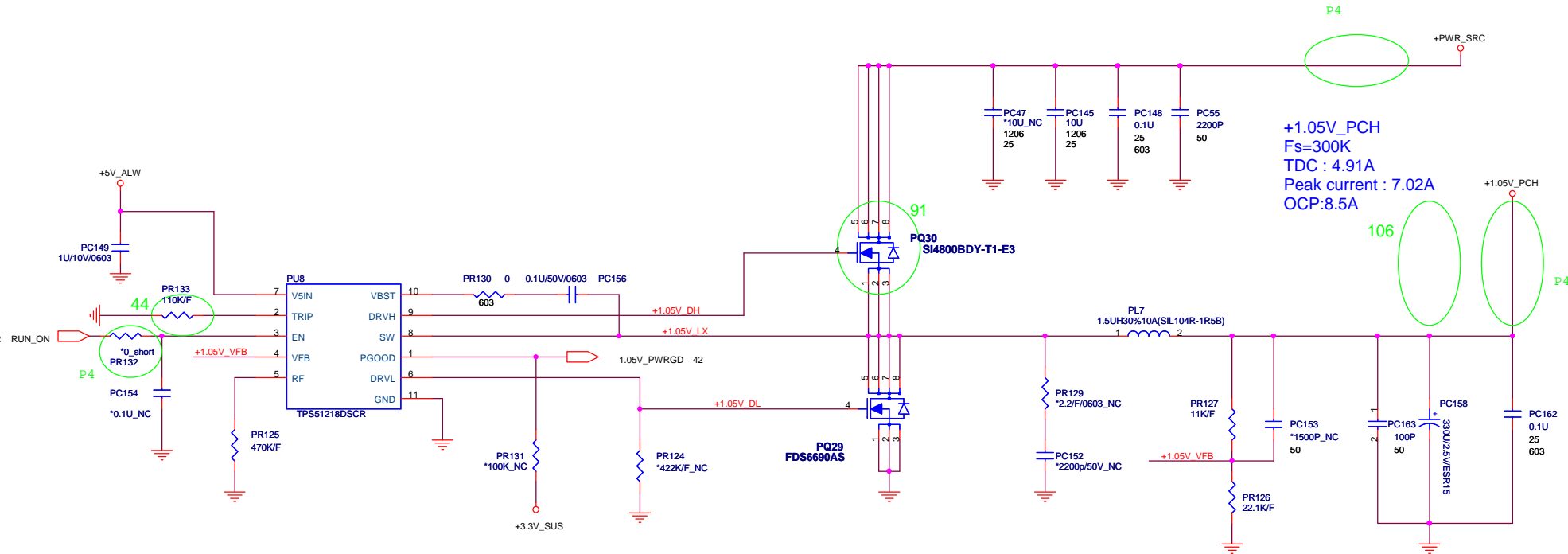
VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	2.5V	VDDQSNS/2	DDR
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

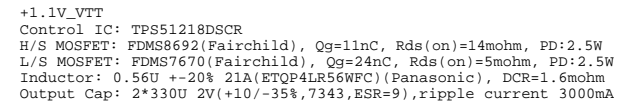
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

D
C
B
A



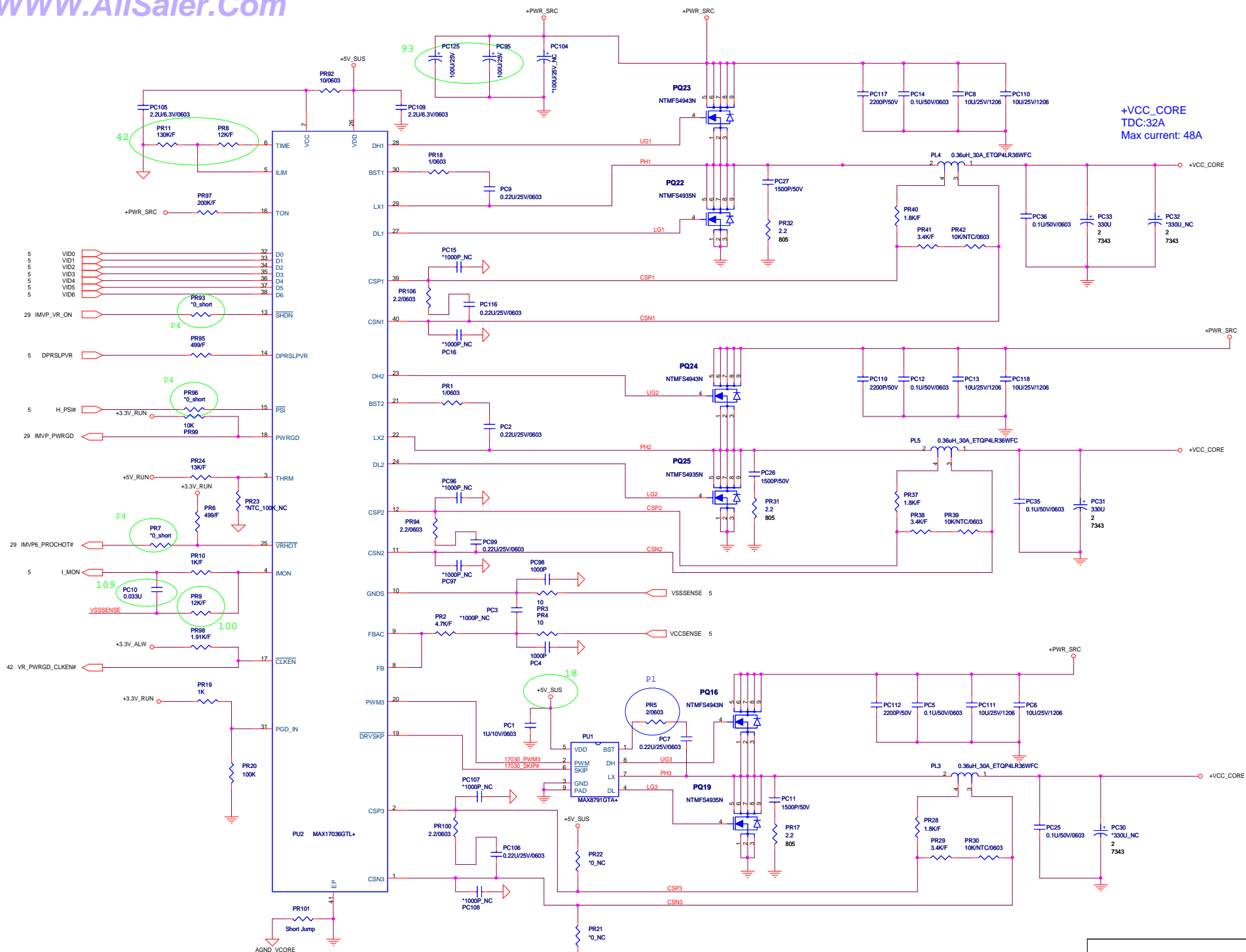
+1.05V_PCH
Control IC: TPS51218DSCR
H/S MOSFET: FDS8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.5W
L/S MOSFET: FDS6690AS(Fairchild), Qg=13nC, Rds(on)=15mohm, PD:2.5W
Inductor: 1.5uH +-30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
Output Cap: 1*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

Title		
+1.05V_PCH(TPS51218)		
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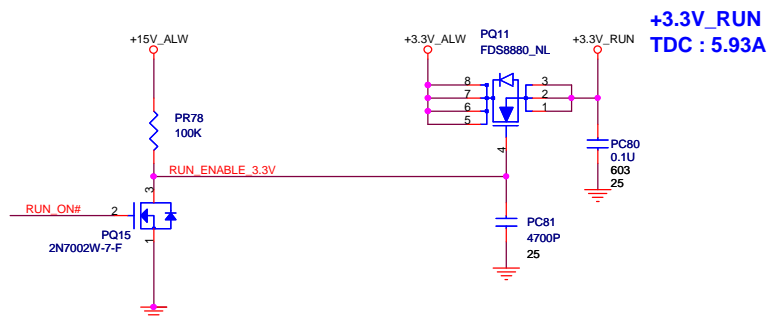
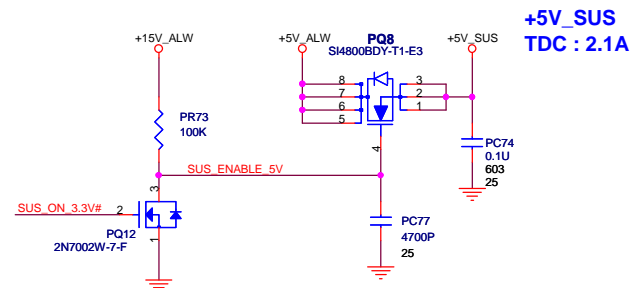
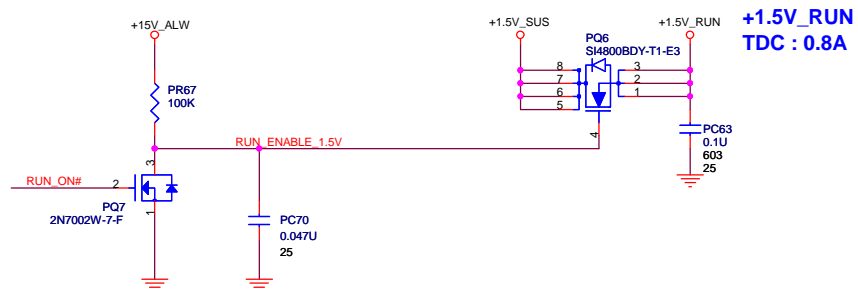
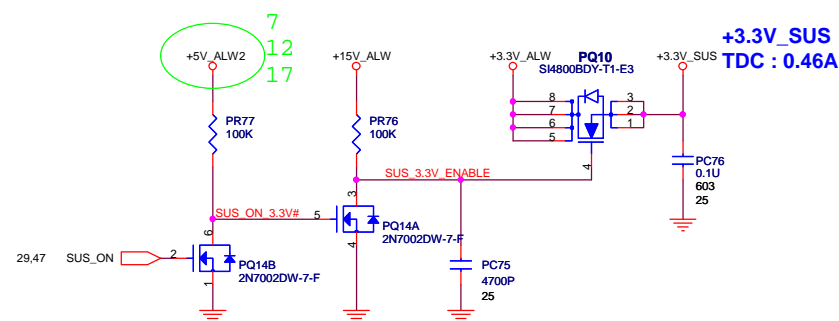
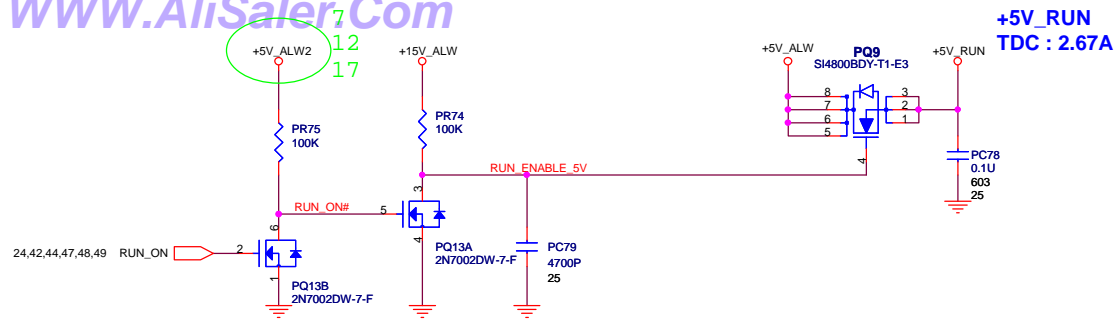


pin5 resister	470kΩ	200kΩ	100kΩ	47kΩ
Frequency	300kHz	350kHz	390kHz	450kHz

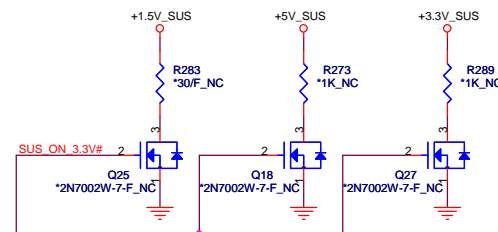
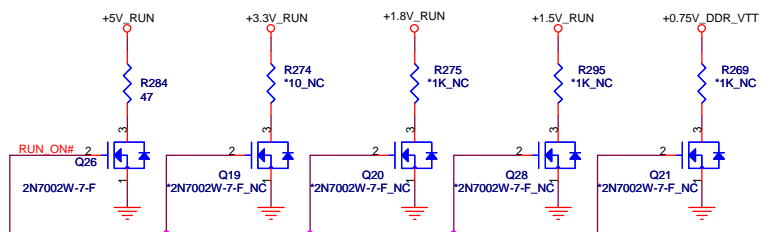
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+1.05V_VTT(TP5S1218)			
Size	Document Number FM9B		Rev 2B
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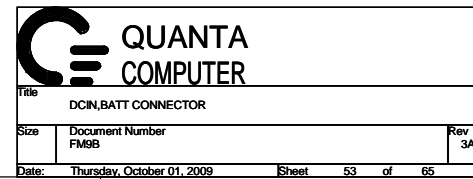
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CPU core (MAX17036)			
Size			
Document Number			
FM93			
Date			
Friday, October 02, 2009			
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28			



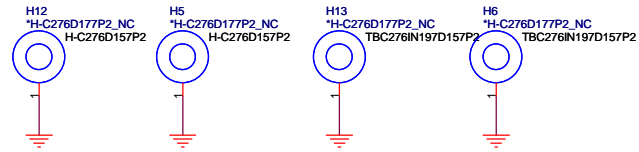
Reserve discharge path



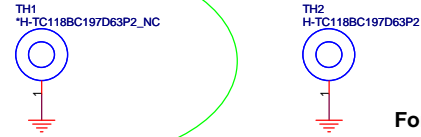
Title		
RUN / SUS POWER SW		
Size	Document Number	Rev
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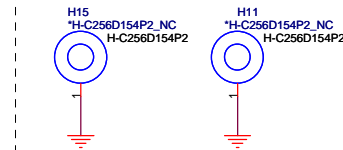
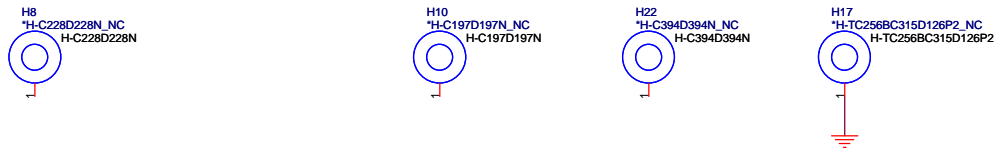
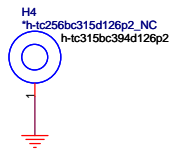
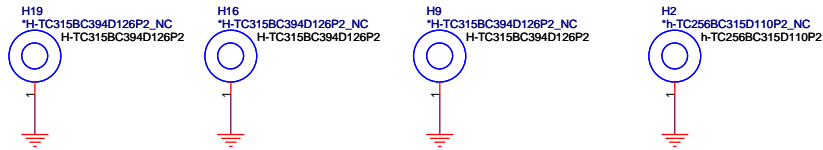
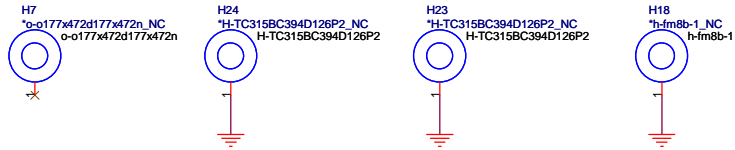
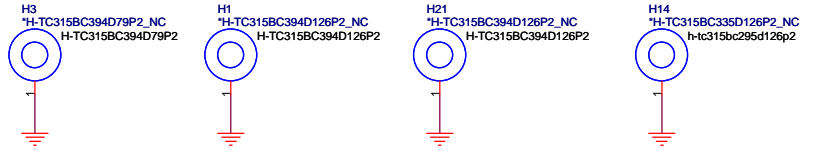
FOR CPU use



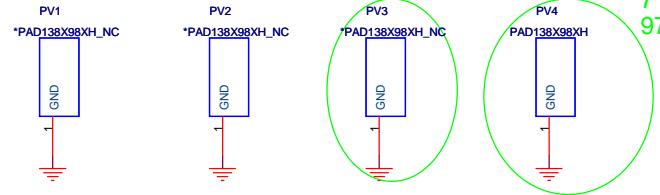
87



For MiniCard nut use.
on 31' header



For PCH nut use.




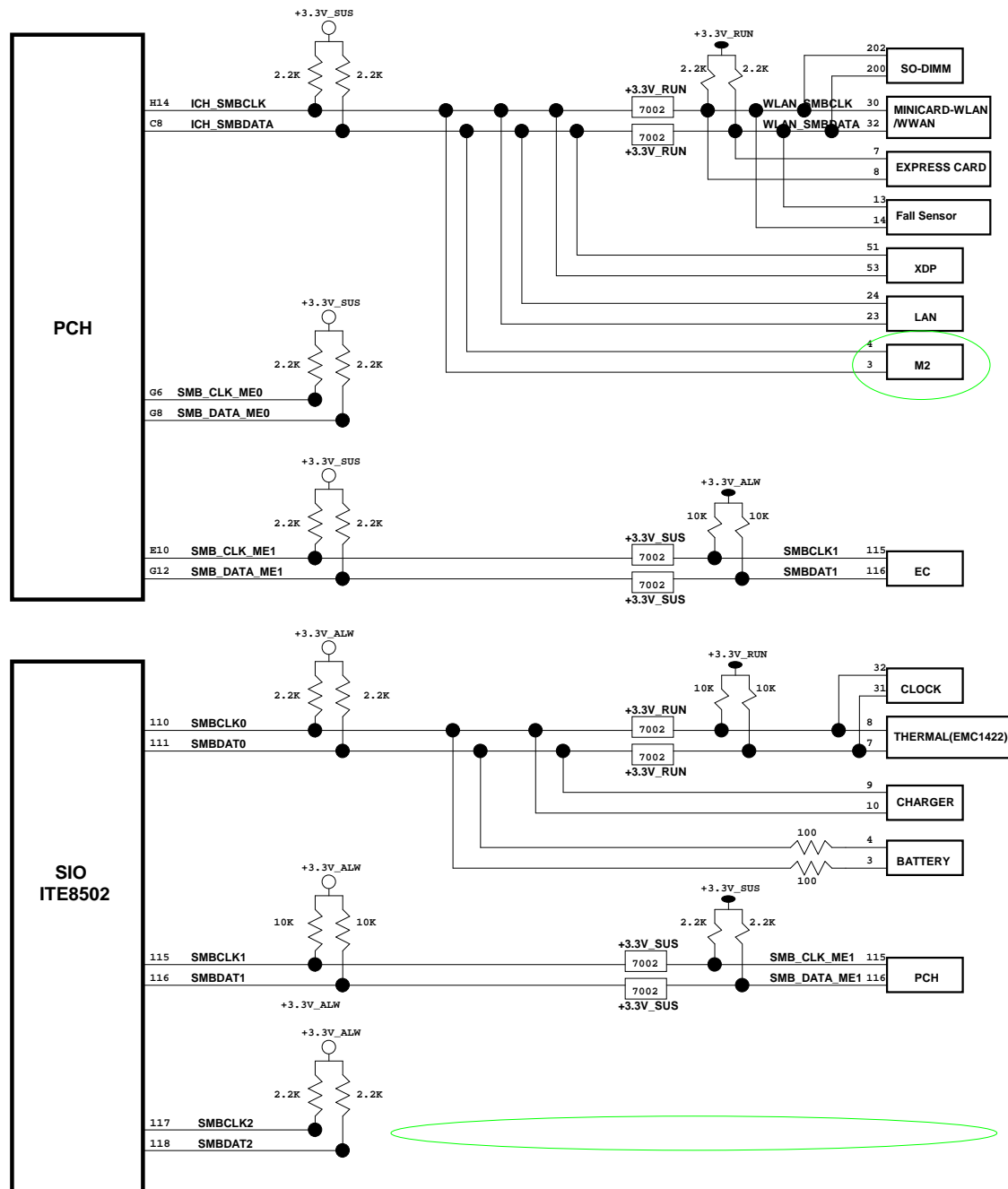
47

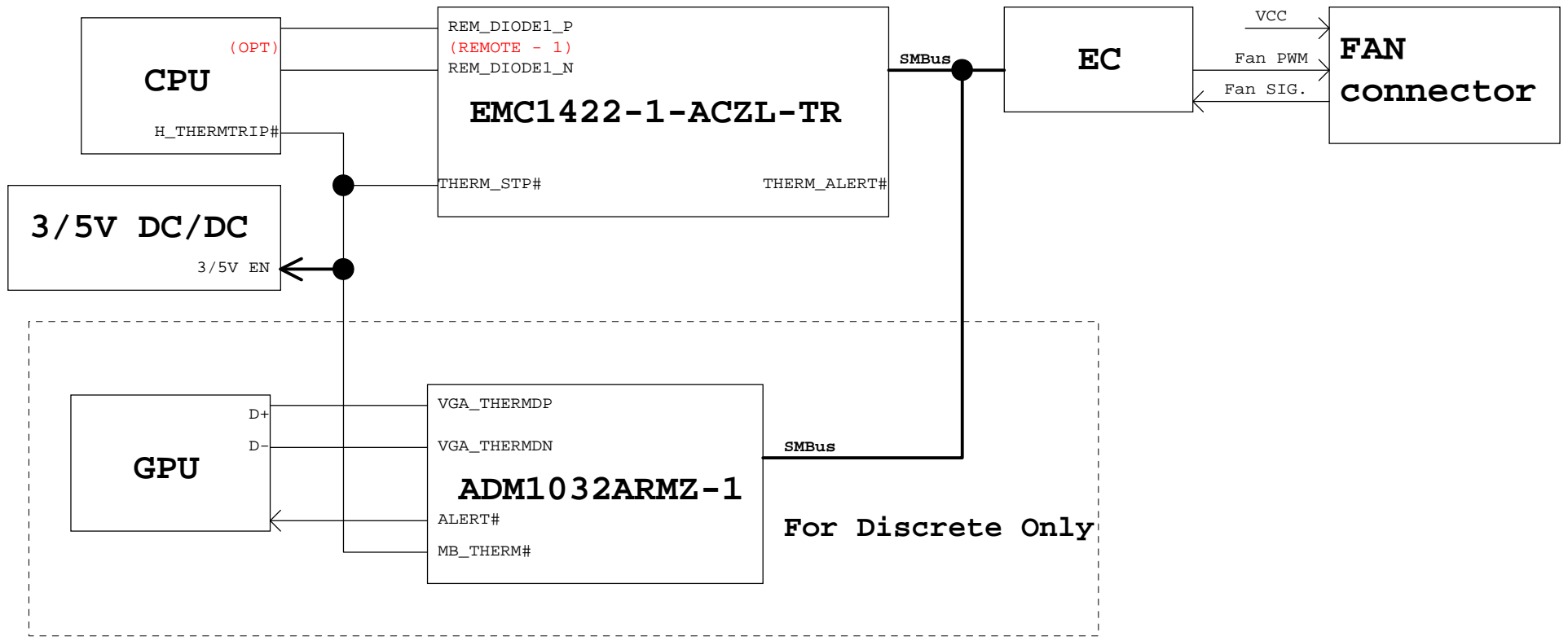
71
97

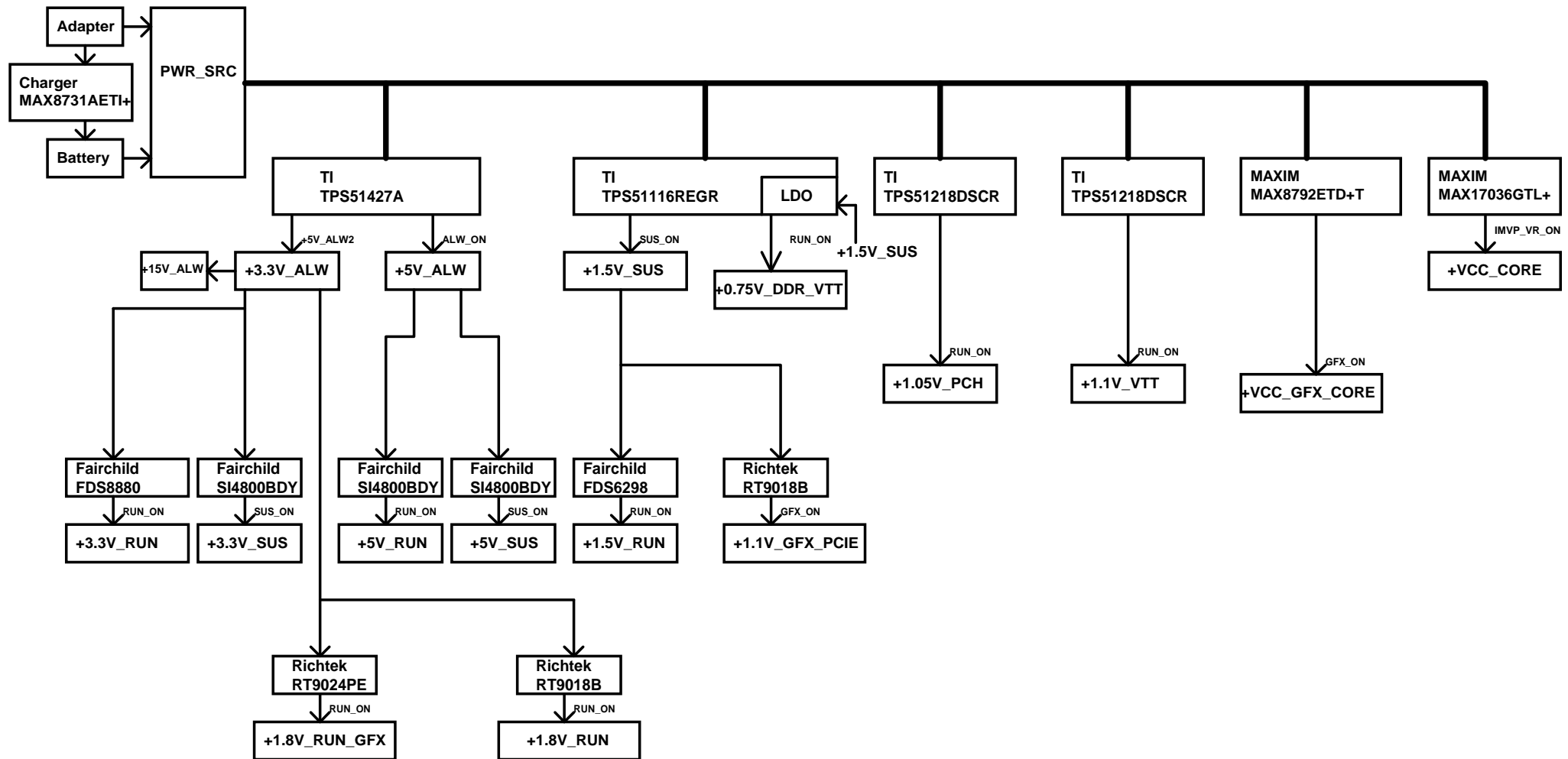


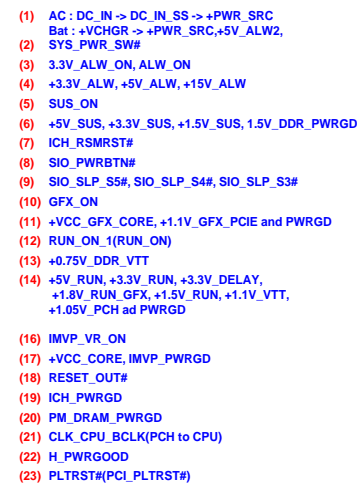
Title			SCREW PAD
Size	Document Number	Rev	
	FM9B	3A	
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 QUANTA COMPUTER		
Title EMI CAP		
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